ELECTROMIGRATION ANALYSIS OF HIGH CURRENT CARRYING ADHESIVE-BASED COPPER-TO-COPPER INTERCONNECTIONS

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ELECTROMIGRATION ANALYSIS OF HIGH CURRENT CARRYING ADHESIVE-BASED COPPER-TO-COPPER INTERCONNECTIONS

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS iii

LIST OF TABLES viii

LIST OF FIGURES ix

SUMMARY xiv

1. INTRODUCTION 1

1.1 More than Moore's Law 2

1.1.1 Trends and Challenges 3

1.2. The Phenomenon of Electromigration 4

1.2.1 Failure Mechanisms of Solder Joints 7

1.3 Electromigration Analysis of Flip Chip Interconnections 10

1.3.1 Gold Stud Bumps 11

1.3.2 Lead-Free Solder 13

1.3.3 Cu pillar with Solder Cap 16

1.3.4 Microbumps 19

1.4 Limitations of Flip Chip Interconnections and Proposed Solution 27

1.4.1 GT-PRC Cu-Cu Interconnections 28

1.5 Thesis Objective 30

1.6 Thesis Outline 30

2. FINITE ELEMENT MODELING OF THREE FLIP CHIP BUMP STRUCTURES 32

2.1 Design Parameters for Bump Structures 32

2.2 Current Crowding and Joule Heating Results 37

2.2.1 Current Crowding Effect 37

2.2.1.1 Peak Current Density 37
2.2.1.2 Current Crowding Ratio 39
2.2.2 Joule Heating Effect 40
2.2.2.1 Joule Heat Generation 40
2.2.2.2 Maximum Bump Temperature 41
2.3 Solder Pillar vs. Cu-Cu 43
2.4 Why is Cu Better than Solder? 45
3. EXPERIMENTAL TEST SETUP 48
3.1 Test Vehicle Design and Fabrication 48
3.1.1 Die Design and Fabrication 48
3.1.1.1 Insulation and Seed Layer 49
3.1.1.2 Metal 1- Dog Bone Layer 50
3.1.1.3 Metal 2- Cu Pillar Bumps 54
3.1.1.4 ENEPIG Surface Finish 56
3.1.1.5 Analysis of the Dog Bone and Bump Structures 59
3.1.2. Substrate Design and Fabrication 61
3.2 Assembly Process for Area-Array Test Vehicle 66
3.3 Electromigration Testing of Cu-Cu Interconnections 67
4. RESULTS AND DISCUSSION 70
4.1 Thermo-mechanical Reliability 70
4.1.1 Initial Assembly Results and C-SAM Inspection 71
4.1.1.1 Root Cause Analysis after Assembly 71
4.1.2 Temperature Cycle Testing 73
4.1.2.1 Root Cause Analysis after TCT 74
4.1.3 Thermo-mechanical Reliability Results 75

4.2 Assembly with Sufficient Load and No Tool Head Tilt 76
4.3 Electromigration Analysis of Cu-Cu Interconnections 79
4.3.1 Electromigration Testing Results 79
4.3.1.1 Current Density Testing at 10^4 A/cm^2, 130°C 79
4.3.1.2 Current Density Testing at 10^5 A/cm^2, 130°C 81
4.3.1.3 Current Density Testing at 10^6 A/cm^2, 130°C 82
4.3.2 Joule Heating Experiment 83
4.4 Cu-Cu Interconnections Discussion 86
5. SUMMARY AND FUTURE WORK 91
5.1 Summary 91
5.2 Future Work 93
REFERENCES 95

LIST OF TABLES

Table 1: ITRS projection of pin-count and pitch for mobile packages [5] 3

Table 2: Electromigration results from AMKOR at maximum current density [16] 22

Table 3: Electromigration analysis of Au stud bumps 23

Table 4: Electromigration analysis of Pb-free solder bumps 24

Table 5: Electromigration analysis of Cu pillar with solder bumps 25

Table 6: Electromigration analysis of microbumps 26

Table 7: Reliability analysis of each chip-last test vehicle [36] 29

Table 8: Material properties used in ANSYS 36

Table 9: Peak current densities of bumps 37

Table 10: Current crowding ratios of bumps 39

Table 11: Joule heat generation of bumps 40

Table 12: Maximum temperature of bumps 42

Table 13: Values for solder pillar structure compared to the Cu-Cu interconnection 43

Table 14: Critical product parameters for Cu and SAC solder 46

Table 15: Parameters for insulation layer 49

Table 16: Parameters for seed layer 50

Table 17: Photolithography parameters of dog bone layer 51

Table 18: Components of the Cu electroplating bath 51

Table 19: Photolithography parameters of Cu pillar bumps 55

Table 20: ENEPIG process steps 57

Table 21: Contents of each component used for ENEPIG surface finish 57

Table 22: Effect of passivation layer on delamination after pre-conditioning 79

Table 23. Benefits of BNUF over NCF 94

LIST OF FIGURES

Figure 1. Schematic illustrating the vision of System-on-Package [3] 2

Figure 2. Current density as a function of bump size [8] 4

Figure 3. Electromigration mass transport in an interconnect line [9] 5

Figure 4. Cycle of void growth due to current crowding and joule heating [10] 8

Figure 5. Current distribution in solder joint when subjected to 0.6A at 100°C through finite element analysis [12] 8

Figure 6. Temperature distribution in solder joint when subjected to 0.6A at 100°C through finite element analysis [12] 9

Figure 7. (a) Cross-section showing asymmetrical dissolution of thick Cu UBM at 125°C and 1.2A of applied current [7]; (b) A schematic showing microstructural evolution at the Cu-Sn interface where Kirkendall voids form [13] 10

Figure 8. Flip chip interconnections: (a) gold stud bumps [14] (b) Pb-free solder [12] (c) Cu pillar with solder cap [15] (d) microbumps [16] 11

Figure 9. Dashed line indicating the location where the wire process would be terminated [17] 12

Figure 10. SEM image after 200 hours of current stress at 3.7A [18] 12

Figure 11. SEM image of Au stud bump with ACA after current stressing [20] 13

Figure 12. Void propagation sequence of a SnAgCu solder at 140°C and $3x10^4$ A/cm^2 at (a) 0 hours, (b) 14 hours, and (c) magnified image of (b) [22] 14

Figure 13. (a) Temperature and (b) current distribution of CuNi UBM versus Cu UBM SAC solder [23] 15

Figure 14. Crowding ratios for each layer of the solder joint for Cu thicknesses of 5μm, 10μm, and 20μm [26] 17

Figure 15. Cross-section showing electromigration failure of Cu pillar with Sn after 300 hours [29] 18

Figure 16. Current density distribution of the Cu and solder region for Cu pillar heights of 1μm, 10μm, 30μm [30] 19

Figure 17. Cross-section of (a) Co-Sn IMC joint and (b) Cu-Sn IMC joint after 1000 hours at 150°C with 300mA of current stress [32] 20

Figure 18. Schematic of chip-last embedded Cu-Cu interconnections [36] 28

Figure 19. ANSYS model of the entire package, which includes a silicon die, BT substrate, and NCF surrounding a single interconnection 33

Figure 20. ANSYS model of Cu-Cu interconnection 33

Figure 21. ANSYS model of Cu pillar with solder cap 34

Figure 22. ANSYS model of Pb-free solder bump 34

Figure 23. Cu pillar with solder interconnection dimensions [37] 35

Figure 24. Vector plots of the electric field for an input current of 1A for the a) Cu-Cu b) Cu pillar with solder and c) Pb-free solder interconnection 36

Figure 25. Plot showing peak current density of each bump 38

Figure 26. Current crowding effect in (a) Cu pillar bump with solder and (b) solder bump [29] 39

Figure 27. Plot showing the current crowding ratio of each bump 40

Figure 28. Plot showing the amount of joule heating in each bump 41

Figure 29. Plot showing maximum temperature of each bump 42

Figure 30. Plot showing each parameter for both the solder pillar and Cu-Cu interconnection 44

Figure 31. Temperature distribution of the a) solder pillar interconnection and b) the Cu-Cu interconnection 44

Figure 32. UBM layers of a flip chip solder bump [4] 46

Figure 33. Close up schematic of Cu-Cu interconnection 47

Figure 34. Test vehicle die design showing bump layout 48

Figure 35. Photoresist mold of the dog bone structure 50

Figure 36. Rack system used to hold wafer through electroplated process 52

Figure 37. 3D laser-confocal profilometry showing ~ 3μm thickness for the dog bone metal layer 53

Figure 38. 3D image of wafers patterned with dog bone layer..... 53

Figure 39. Process flow for 6” wafer fabrication..... 55

Figure 40. Optical microscope image of a single die with ENEPIG surface finish..... 58

Figure 41. Optical microscope image at 50X focused on the (a) 30μm bumps and (b) the dog bone..... 59

Figure 42. A 3D microscope image of the dog bone layer with Cu pillar from a (a) side view and (b) top view 59

Figure 43. A 3D microscope image showing an average roughness of ~1μm for the Cu pillars..... 60

Figure 44. Images of 3D laser-confocal profilometry showing (a) dog bone and (b) Cu pillar height 60

Figure 45. SEM images of a dog bone and Cu pillar bump (a) with ENEPIG and (b) without ENEPIG 61

Figure 46. Substrate design showing 24 probe pads and 16 daisy chains 61

Figure 47. Stack-up layer inside of hot press to laminate RXP-4 build-up layers on RXP-1 core..... 63

Figure 48. Process flow showing fabrication process for 6in x 6in substrate panels of RXP and BT..... 64

Figure 49. Optical microscope image of the four corners of the test vehicle substrate coupon using BT 64

Figure 50. Optical microscope image of (a) probe pads and (b) traces leading to a center daisy chain of the test vehicle substrate coupon using BT 65

Figure 51. Optical microscope image of the four corners of the test vehicle substrate coupon using RXP 65

Figure 52. Optical microscope image of (a) probe pad and (b) traces leading to a center daisy chain of the test vehicle substrate coupon using RXP..... 65

Figure 53. Process flow for assembly of area-array test vehicle 66

Figure 54. Temperature profile used during thermo-compression bonding 67

Figure 55. Manual test setup for current density testing at 10^4 A/cm^2 68

Figure 56. Automatic test setup for current density testing at 10^5 A/cm^2..... 68

Figure 57. Manual test setup for current density testing at 10^6 A/cm^2 69

Figure 58. Process flow used to examine the Cu-Cu interconnections for thermo-mechanical reliability 70

Figure 59. Test vehicle daisy chain layout with die and substrate aligned 71

Figure 60. Cross-section of partially-yielding die showing (a) no deformation on the left edge and (b) proper bump-to-pad deformation on the right edge 72

Figure 61. C-SAM image of BT assembly (a) without NCF dry-up process and (b) with NCF dry-up process and IPA cleaning 73

Figure 62. C-SAM image of BT assembly (a) after thermo-compression bonding and (b) after 500 cycles of TCT 73

Figure 63. C-SAM image of RXP assembly (a) after thermo-compression bonding and after (b) 500 cycles of TCT 74

Figure 64. Cross-section of a BT assembly showing delamination between silicon die and NCF after TCT 74

Figure 65. Normalized daisy chain resistances of test vehicle with RXP for 2000 cycles 75

Figure 66. Normalized daisy chain resistances of test vehicle with BT for 2000 cycles . 75

Figure 67. Process flow using BT substrates and NCF at Namics Corporation 76

Figure 68. Temperature profile used during thermo-compression bonding at Namics Corporation 76

Figure 69. Final BT assemblies with good electrical yield and no voiding (red circles show missing bumps from the die side due to fabrication defects) 77

Figure 70. Cross-sectional image showing proper bump-to-pad deformation of a BT assembly with NCF 77

Figure 71. C-SAM images of BT samples after assembly and pre-conditioning 78

Figure 72. Cross-sectional analysis of BT assembly showing delamination between silicon die and NCF after pre-conditioning 78

Figure 73. Plot showing area-array sample surviving ~800 hours at 10^4 A/cm^2 with an improvement in resistance over time 80

Figure 74. Plot showing area-array sample surviving >2800 hours at 10^5 A/cm^2 with an improvement in resistance over time 81

Figure 75. Plot showing peripheral interconnection sample surviving >1100 hours at 10^6 A/cm^2 with an improvement in resistance over time 82

Figure 76. Image showing burned polymer around Cu trace after applying 10^7 A/cm^2 current density 83

Figure 77. Overlapped die and substrate design showing the single corner bump which current was applied to 84

Figure 78. IR image of the sample displaying emissivity and the different structures such as the Cu bumps and Cu traces 84

Figure 79. The increase in bump temperature due to joule heating with respect to the applied current 85

Figure 80. ANSYS model showing temperature distribution of 15µm diameter Cu bump 86

Figure 81. (a) Image showing disappearance of the bonding interface after Cu-Cu thermo-compression bonding at room temperature and high load; (b) Graph showing measured shear strengths at different bonding temperatures [67] 88

Figure 82. After Cu-Cu bonding at 300°C and annealing at 400°C, a homogenous layer was obtained through diffusion and grain growth [70] 88

Figure 83. (a) Distinguishable Cu-Cu interface observed after bonding at 300°C which (b) disappears after a 300°C annealing step [71] 89

Figure 84. Morphology and strength map for Cu wafer bonding under different bonding temperatures and conditions [72] 89

Figure 85. Percentage of failed dies at different bonding conditions after dicing [72] 90

SUMMARY

"More Than Moore's Law" is the driving principle for the electronic packaging industry. This principle focuses on system integration instead of transistor density in order to achieve faster, thinner, and smarter electronic devices at a low cost. A core area of electronics packaging is interconnection technology, which enables ultra-miniaturization and high functional density. Solder bump technology is one of the original, and most common interconnection methods for flip chips. With growing demand for finer pitch and higher number of I/Os, solder bumps have been forced to smaller dimensions and therefore, are subjected to higher current densities. However, the technology is now reaching its fundamental limitations in terms of pitch, processability, and current-handling due to electromigration.

Electromigration in solder bumps is one of the major causes of device failures. It is accelerated by many factors, one of which is current crowding. Current crowding is the non-uniform distribution of current at the interface of the solder bump and under-bump metallurgy, resulting in an increase in local current density and temperature. These factors, along with the formation of intermetallic compounds, can lead to voiding and ultimately failure. Electromigration in solder bumps has prevented pitch-scaling below 180-210μms, producing a shift in the packaging industry to other interconnection approaches, specifically copper pillars with solder.

This research aims to explore the electromigration resistance of an adhesive-based copper-to-copper (Cu-Cu) interconnection method without solder, which is thermo-compression bonded at a low temperature of 180°C. While solder bumps are more susceptible to electromigration, Cu is capable of handling two orders of magnitude higher current density. This makes it an ideal candidate for next generation flip chip interconnections.

Using finite element analysis, the current crowding and joule heating effects were evaluated for a 30μm diameter Cu-Cu interconnection in comparison with two existing flip chip interconnection techniques, Cu pillar with solder and Pb-free solder. A test vehicle (TV) was fabricated for experimental analysis with 760 bumps arranged in an area-array format with a bump diameter of 30μm. Thermo-mechanical reliability of the test vehicle was validated under thermal cycling from -55°C to 125°C. The Cu-Cu interconnections were then subjected to high current and temperature stress from 10^4 to 10^6 A/cm^2 at a temperature of 130°C. The results establish the high thermo-mechanical reliability and high electromigration resistance of the proposed Cu-Cu interconnection technology.

CHAPTER 1

INTRODUCTION

The modern world has changed dramatically due to the advancement of electronics. Our daily opportunities have increased because of devices that allow us to navigate through unfamiliar roads, video chat with family across the world, and monitor blood pressure while reporting the data wirelessly to our physician. All these and others are made possible by advances in transistor scaling and package miniaturization technologies, resulting in small portable handheld devices.

Electronics packaging is a multifaceted area of engineering that allows for constant progression towards ultra-miniaturization, higher functionality and low cost. The integrated circuit (IC) is the backbone of all electronic devices, but electronics packaging goes beyond to connect these ICs with other components in order to create an entire functional system. There are four different functions of packaging including (1) signal distribution, (2) power distribution, (3) heat dissipation, and (4) protection [1].

This thesis focuses on first-level packaging, specifically the interconnect system which connects the IC to the package, and how the trend for high functionality at small form factor has introduced the need for an interconnection technique that can be implemented at ultra-fine pitch, low stand-off height, and high I/O density. However, the problem in this movement is the interconnection reliability concerns that arise in meeting this demand. A major issue associated with small interconnection dimensions is the phenomenon of electromigration, which produces failures due to high current densities. Georgia Tech Packaging Research Center (GT-PRC), with its continuous drive towards advancements in packaging, has overcome electromigration related barriers for high density applications by demonstrating a robust all-copper interconnection system with high thermo-mechanical reliability and current carrying capability. This chapter discusses

the semiconductor industry's roadmap for the future and how that motivates the development of the proposed electromigration resistant interconnection technique.

1.1 More than Moore's Law

Moore's Law states that the number of transistors per square inch on an IC will double every 18 months. Currently, the semiconductor industry is in the 22nm node and is expected to surpass this in the coming years. Even though the growing number of transistors increases processing speed and performance of computers, Moore's Law only concentrates on integration at IC level and does not consider overall system functionality or its miniaturization. To address these challenges, GT-PRC began to pioneer the concept of System-on-Package (SOP) where device, package, and system board are all miniaturized for next generation convergent systems. Convergent systems revolutionize electronic devices by merging computer, communications, consumer and even biomedical functions into one portable product [2].

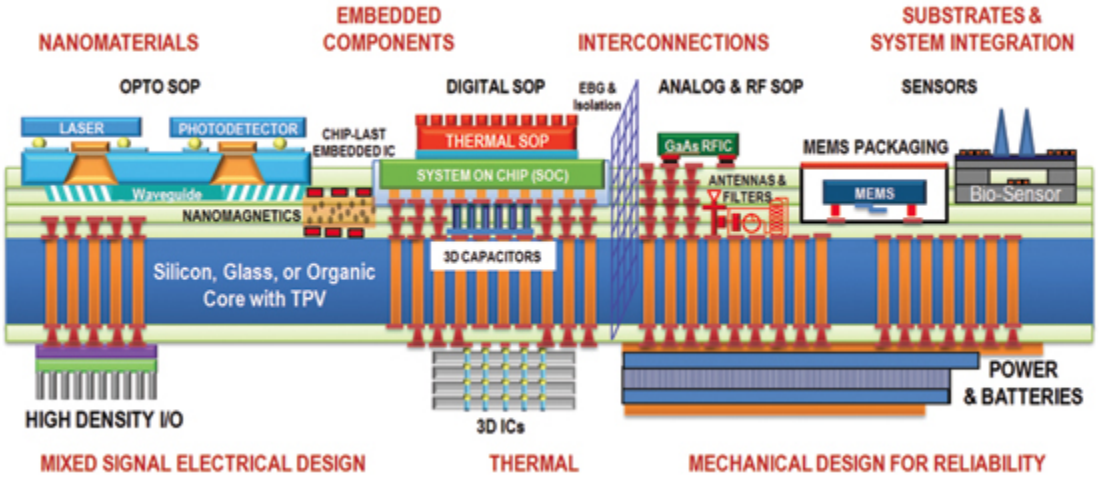


Figure 1. Schematic illustrating the vision of System-on-Package [3]

The vision behind SOP became the basis for the "Second Law of Electronics" which scales and integrates all system components such as passive components, interconnections, thermal structures, and system board. The SOP thus utilizes the best of on-chip and off-chip integration to allow for ultra-miniaturization, high performance,

high reliability, and low cost [3]. In order to support the goal of SOP, flip chip technology was employed due to its high reliability, superior electrical performance, and reparability. The flip chip process involves turning the IC upside down with the active side facing down and bonding it to a chip carrier or substrate. With wire bonding being limited to peripheral contacts, flip chip technology allows for the entire surface of the die to be used for interconnects, which means higher I/O density and smaller chip size [4].

1.1.1 Trends and Challenges

The International Technology Roadmap for Semiconductors (ITRS) projects 1150 I/Os at 95µm area-array pitch for mobile packages by 2017, as seen from Table 1 [5]. This increasing trend in I/O density requires a flip chip interconnection technique that can be implemented at ultra-fine pitch, low stand-off height, while withstanding high current densities in order to meet power requirements at smaller sizes.

Table 1: ITRS projection of pin-count and pitch for mobile packages [5]

Projected Flip Chip Pin-Count and Pitch Size						
Year of Production	**2012**	**2013**	**2014**	**2015**	**2016**	**2017**
Package Pin-count Maximum	188-1000	198-1050	207-1100	218-1150	218-1150	240-1150
Flip Chip array pitch (µm)	110	110	100	100	100	95

IBM introduced the Controlled Collapsed Chip Connection process (C4) in 1964 using solder bumps and major advancements have been made since then to meet the demands of the semiconductor industry. These technological advancements focus on overcoming fabrication and reliability concerns that occur at smaller dimensions such as underfilling between chip and package, high fatigue at low stand-off heights, and solder bridging at fine pitch. Of all these issues, however, one of the key factors limiting pitch-scaling below 180µm for solder bumps is the phenomenon of electromigration. Electromigration induces failures within the bump due to increased current density at

small dimensions and fine pitch. Decreasing the bump diameter from 200µm to 50µm increases the current density 16 times, as depicted in Figure 2. Currently, solder-based flip chips are required to handle 0.2A of current per bump, but this is expected to double in the near future [6]. According to Table 1, the expected bump pitch of 100µm by 2014 demands the solder bump diameter to be about 50µm. This decrease in bump diameter dramatically increases the current density per solder bump to 10^4 A/cm^2, which is considered the electromigration threshold for solders [7].

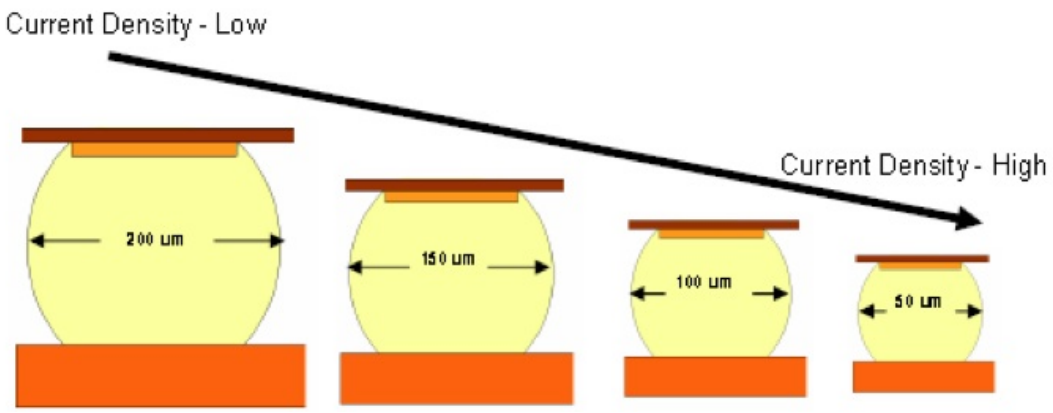


Figure 2. Current density as a function of bump size [8]

1.2. The Phenomenon of Electromigration

Electromigration is known as enhanced atomic displacement within a conductor due to an applied electric current. This phenomenon is a huge concern as increased atomic displacement causes a reduction in reliability through a polarity effect where atoms accumulate at the anode end, causing short circuits, and vacancies occur at the cathode end, causing open circuits [9]. Electromigration happens through diffusion under an electrical driving force. Einstein's equation of atomic flux, J_a, can be related to this driving force, F, where C_a is the atomic concentration and μ is the mobility of atoms [10]:

$$J_a = C_a \mu F \qquad (1)$$

This driving force, F, can be expanded into two contributing factors: a direct force and an electron wind force. The direct force is proportional to the applied electric field, E, and goes in the direction of the field. The electric field also accelerates conduction electrons that tend to scatter at places of imperfections within the lattice, such as vacancies, grain boundaries, and dislocations [10]. This scattering causes a momentum shift to the metal ions which exerts a force proportional to the electric field intensity, called the electron wind force, in the direction opposite to the electric field [9]. Thus, the net driving force is equivalent to these two forces where Z^*e is the effective charge of the metal ions, j is the current density, and ρ is the resistivity of the metal [10]:

$$F_{net} = F_{direct} + F_{wind} = (Z_d + Z_w)ej\rho = Z^* ejp \quad (2)$$

In metals, such as Cu, F_{net} is dominated by the electron wind force and thus the atomic flux goes in the direction opposing the electric field [9].

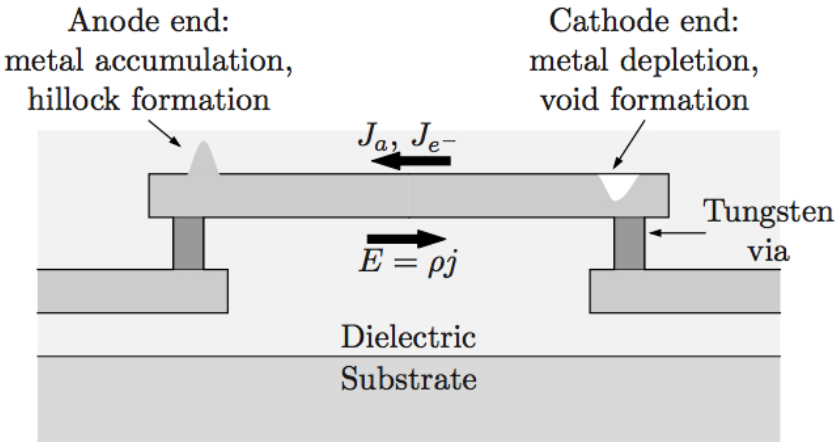


Figure 3. Electromigration mass transport in an interconnect line [9]

To further dissect the atomic flux equation, the mobility of atoms can be expressed in terms of atomic diffusivity, D, and thermal energy, kT [10]:

$$\mu = \frac{D}{kT} \qquad (3)$$

Combining Equations 2 and 3 results in the final atomic flux equation for electromigration:

$$J_a = -\frac{C_a D Z^* ej\rho}{kT} \qquad (4)$$

When electromigration occurs at steady-state, there is no change in atomic concentration and no failures occur. Once there is divergence in the atomic flux, then failures will start to transpire. For example, if the atomic flux into a region is greater than the flux leaving it, mass accumulation occurs and hillocks form. If the flux leaving a region is greater than the flux entering it, mass depletion occurs and voids form. The voids are detrimental because the cross-sectional area of the conductor begins to decrease, resulting in an increase in current density and resistance. The contributing factors to flux divergence include variation in microstructure, material composition, and temperature [10].

The variation in microstructure of the material plays a critical role in electromigration and involves differences in the grain size or orientation, atomic diffusivity, and chemical composition. Specifically, electromigration is strongly affected by grain structure. For example, the grain boundaries in Aluminum (Al) have lower activation energy than in the bulk region, meaning they contain fewer obstacles for diffusion. Therefore, the diffusion rate is faster at grain boundaries and the overall rate of atomic transport in Al is dependent on the grain size [10].

The material properties can affect electromigration due to the differences in diffusion rate between the various materials within an electronic package, which cause atomic flux divergence at the interface between them. Mass accumulation occurs in a region where the current goes from a material with high diffusivity to a material with low diffusivity. Conversely, void formation occurs when current flows from low to high diffusivity materials [10].

Diffusion is also dependent on temperature, which can be seen from the equation below where D_o is the maximum diffusion coefficient, E_A is the activation energy, k is the gas constant, and T is the temperature in Kelvins:

$$D = D_o \exp(-\frac{E_A}{kT}) \qquad (5)$$

As temperature increases, the diffusion rate also increases. Therefore, any difference in temperature enhances the possibility of void and hillock formation. One of the major causes of electromigration failure is local heating within interconnects, which occurs due to current crowding [10].

In 1969, J. R. Black developed a model to predict the mean-time-to-failure of an Al interconnect due to electromigration. The Black's model suggests that the lifetime of an interconnection is dependent on temperature and current density:

$$MTTF = AJ^{-n} \exp(\frac{E_A}{kT}) \qquad (6)$$

In this equation, A is a constant that is dependent on the material, J is the applied current density, n is the current density exponent, and as previously mentioned, E_A, k, T is the activation energy, gas constant, and temperature, respectively. In order to determine the mean-time-to-failure (MTTF), samples are subjected to extreme current and temperature conditions until 50% of the sample has failed [11].

1.2.1 Failure Mechanisms of Solder Joints

There are common behaviors that induce electromigration failures in solder joints, such as current crowding and joule heating. When flux divergence causes voids to form, the cross-sectional area within the bump is reduced. Accordingly, this creates an increase in local current density, known as current crowding, which causes joule heating to occur. A continuing cycle takes place where an increase in local temperature, due to joule heating, increases the rate of local atomic migration and flux divergence. This in turn accelerates the rate of electromigration damage through voiding. As void growth is accelerated, the electronic device eventually develops an open circuit.

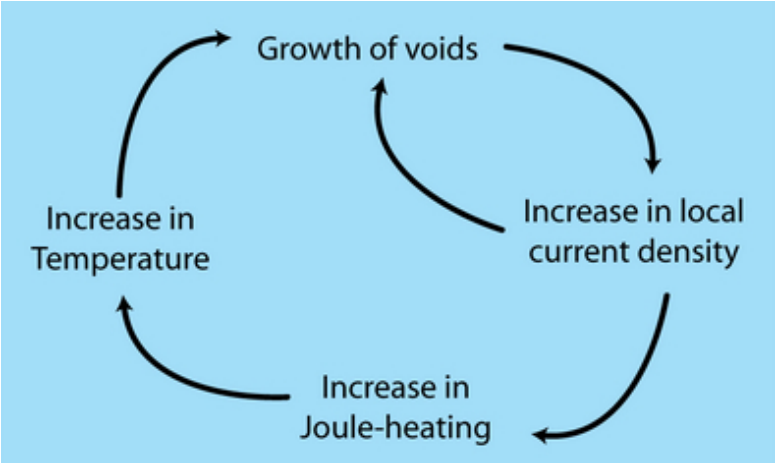


Figure 4. Cycle of void growth due to current crowding and joule heating [10]

The main cause of current crowding in flip chip solder joints is the line-to-bump configuration of the thin film trace and solder bump. A three-dimensional simulation by K. N. Tu et al. [12] demonstrated that the difference in cross-sectional area between the Al trace on the chip side and the solder bump caused an increase in local current density. Figure 5 reveals that the current density near the entrance of the solder bump was approximately one order of magnitude higher than the average current density in the middle of the bump [12].

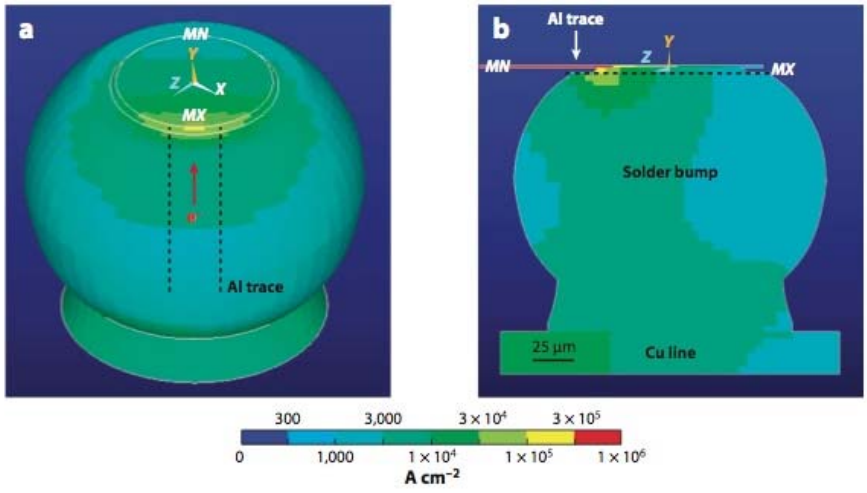


Figure 5. Current distribution in solder joint when subjected to 0.6A at 100°C through finite element analysis [12]

As previously mentioned, current crowding causes an increase in local bump temperature, known as joule heating. As moving electrons collide with atoms in a conductor, the momentum shifts to the atoms and increases their kinetic energy in the form of heat [10]. The joule heating power, P, is dependent on current density J, resistivity ρ, and volume v:

$$P = J^2 \rho v \qquad (7)$$

K. N. Tu et al. [12] also used three-dimensional simulation to investigate joule heating. The resistance of the Al trace was determined to be hundreds of milliohms, while the solder bump was around 7mΩ. This drastic difference in resistance, in addition to the volume of the trace being much smaller than the bump, resulted in the Al trace having three magnitudes higher joule heating than the solder bump. Once again, a hot spot was found at the entrance point where electrons flow from the Al trace into the solder bump, as seen in Figure 6. The temperature of the hot spot was 137.4°C, which was 5.6°C higher than the average temperature of the bump [12].

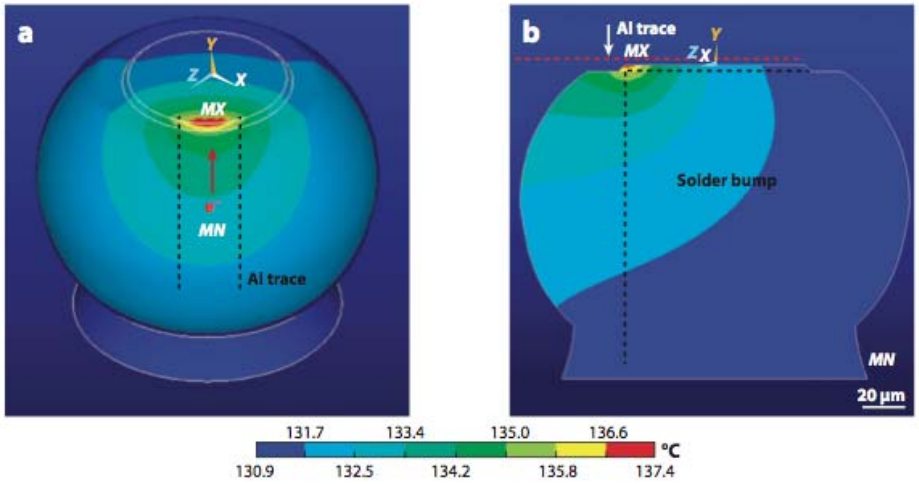
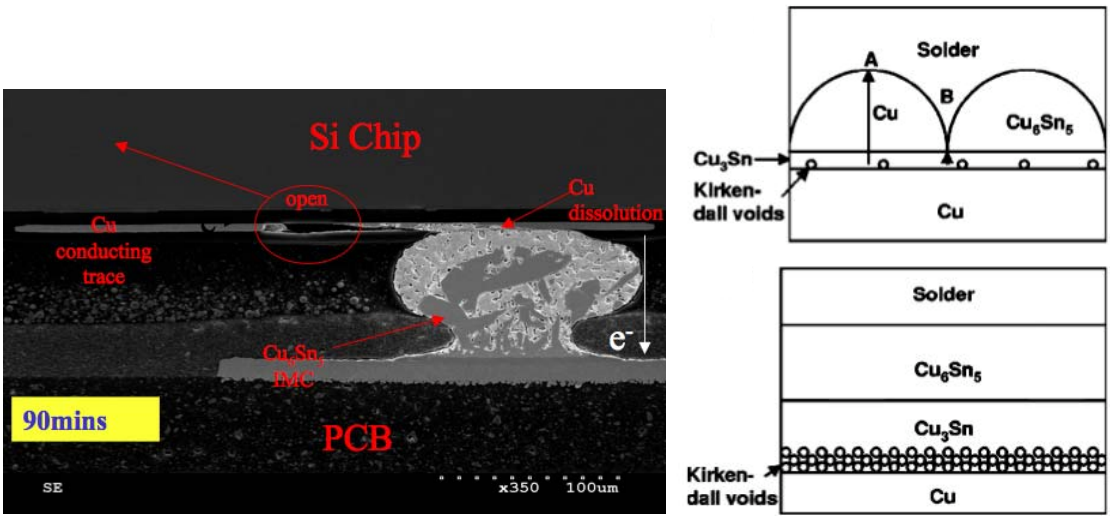


Figure 6. Temperature distribution in solder joint when subjected to 0.6A at 100°C through finite element analysis [12]

Another failure mechanism that occurs due to electromigration is dissolution of the UBM which can create open circuits. Two common materials used for the UBM

structure are Cu and Ni and large amounts of each gets dissolved to form intermetallic compounds (IMC) within the bump. The diffusion rate is really fast for noble and near-noble metals (Cu, Ag, Au, Ni, Pd, Pt) since they diffuse interstitially in group IV elements (Si, Ge, Sn, Pb). Due to the polarity effect mentioned earlier, UBM dissolution occurs at the cathode end and IMC formation occurs at the anode end [7]. IMC formation over time also creates sub-micron voids called "Kirkendall voids" that can facilitate initial crack propagation. For Cu UBM, Kirkendall voids are found in the Cu_3Sn layer, as shown in the schematic below [13].



(a) **(b)**

Figure 7. (a) Cross-section showing asymmetrical dissolution of thick Cu UBM at 125°C and 1.2A of applied current [7]; (b) A schematic showing microstructural evolution at the Cu-Sn interface where Kirkendall voids form [13]

1.3 Electromigration Analysis of Flip Chip Interconnections

After the development of C4 technology using tin-lead (SnPb) solder, many variations of flip chip joints were introduced to reduce cost, overcome environmental concerns through lead-free processes, and most importantly to enable fine-pitch. This brought into the industry an assortment of flip chip interconnections including: gold stud bumps, lead-free solder, Cu pillar with solder cap, and microbumps. Considering the huge impact of electromigration at smaller bump sizes, a thorough analysis of all four

technologies under current and temperature stress has been evaluated. In order to assess the electromigration resistance of GT-PRC's Cu-Cu interconnection technique, the current status of existing interconnections needs to be fully understood.

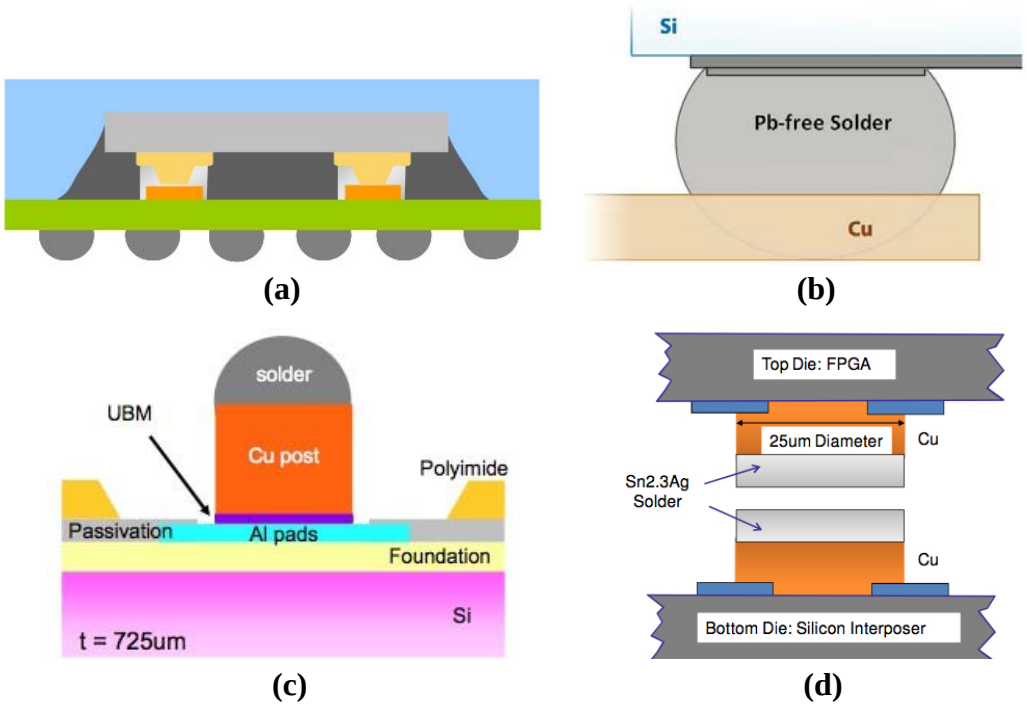


Figure 8. Flip chip interconnections: (a) gold stud bumps [14] (b) Pb-free solder [12] (c) Cu pillar with solder cap [15] (d) microbumps [16]

1.3.1 Gold Stud Bumps

Gold stud bumping was introduced as a low cost solution to reach fine pitches of 50µm. The process includes using existing wire bonding techniques to make a connection from the IC to the substrate. However, the wire is snapped off after a gold ball is thermosonically bonded to the die bond pad. Figure 9 shows a typical wire connection and a dotted line indicating where the wire is cut. After the gold stud is created, the die is then bonded to the substrate using many techniques such as anistropic conductive films (ACF), conductive epoxy, thermo-compression bonding, and ultrasonic bonding [17].

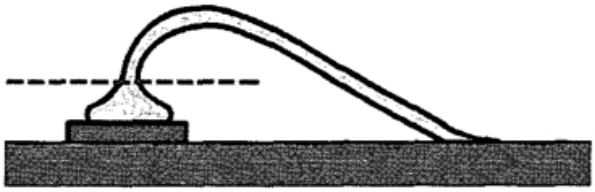


Figure 9. Dashed line indicating the location where the wire process would be terminated [17]

Gold is an excellent electrical conductor and therefore has excellent current carrying capability. While investigating the reliability of Au stud bumps under high current stress, W.S. Kwon et al. [18] revealed 85μm diameter Au stud bumps with ACF having a predicted lifetime of 25 years at a current density of $5x10^4$ A/cm^2. However, once the current density was increased to $7x10^4$ A/cm^2, the lifetime severely decreased to 12.28 hours. Kwon et al. also conducted failure analysis and concluded four different types of failure mechanisms after current stressing: 1) formation of Au-Al compounds due to joule heating 2) Al depletion 3) crack formation between the Au-Al IMC and stud bump and 4) adhesive delamination.

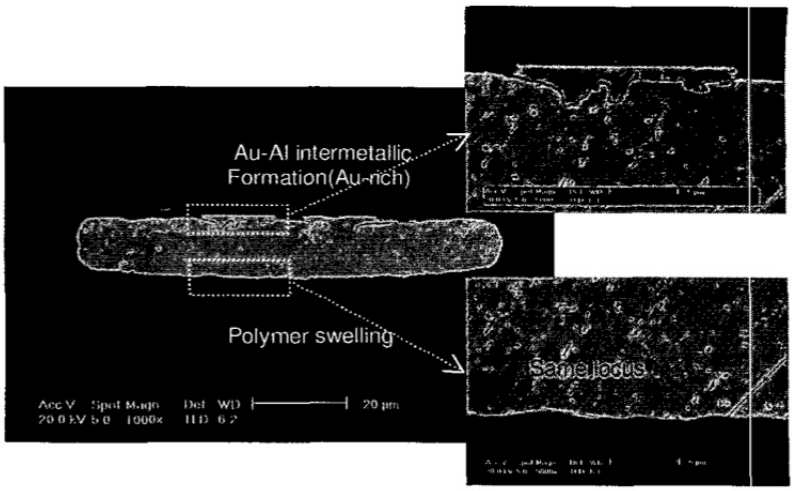


Figure 10. SEM image after 200 hours of current stress at 3.7A [18]

Another study by M. J. Yim et al. [19-20] explored the degradation mechanism and reliability of thermally-conductive anisotropic conductive adhesives (ACA) with 85μm Au stud bumps under current stress. He claimed that high current densities caused

failures because of: 1) interface degradation between the non-solder bump and I/O pad metal due to IMC formation and 2) delamination and adhesive swelling due to joule heating.

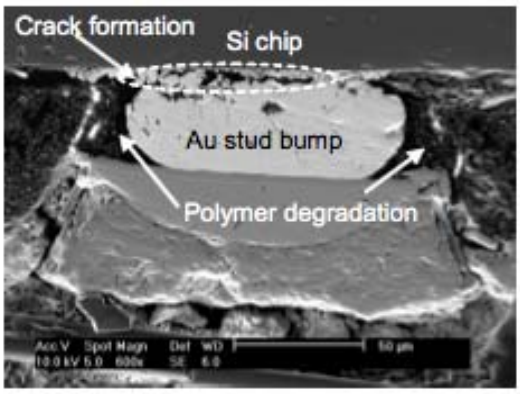


Figure 11. SEM image of Au stud bump with ACA after current stressing [20]

Yim et al. suggested that the high junction temperature of adhesive flip chip joints could be mitigated with the use of thermally-conductive fillers in the ACA which would provide proper heat dissipation. The research indicated that the current carrying capability was improved from 3.6A to 6.7A by using thermally conductive ACA with 5μm Ni and 0.2μm silicon carbide (SiC) fillers. However, only 3A of current stress, or $5x10^4$ A/cm^2 current density, was reported for 200 hours without failure. It can be concluded that the maximum current density tested for Au stud bumps with ACF/ACA is around 10^4 A/cm^2. There have been no reported cases of simultaneous current and temperature stressing.

1.3.2 Lead-Free Solder

Solder joints have primarily been composed of Sn and Pb since the start of the electronics industry. However, due to the harmful effects of lead, the European Union initiated the "Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment" which spearheaded the movement towards lead-free devices in 2003. A common alloy in the industry that has replaced SnPb solder is tin-

silver-copper (SnAgCu) or SAC [21]. With the adoption of this new material, research has been conducted to understand the lifetime of these joints under extreme current and temperature conditions. Choi et al. [22] in 2003 explored the MTTF of SnPb solder and SAC solder at 125µm diameter. The maximum current density and temperature applied to the SnPb solder and SAC solder was $2.75x10^4$ A/cm^2 at 140°C and $3x10^4$ A/cm^2 at 160°C, respectively. The MTTF for these extreme cases was 1 hour for the SnPb solder and 2 hours for the SAC solder. When both bumps were put under the same conditions of 2.25×10^4 A/cm^2 at 125°C, the SnPb solder lasted only 43 hours whereas the SAC solder lasted for 580 hours. The figure below shows a SEM image of a void propagation sequence for the SAC bump after 14 hours at $3x10^4$ A/cm^2 and 140°C. The study concluded that the fast failure rate for both types of solder was due to current crowding, joule heating, and IMC dissolution.

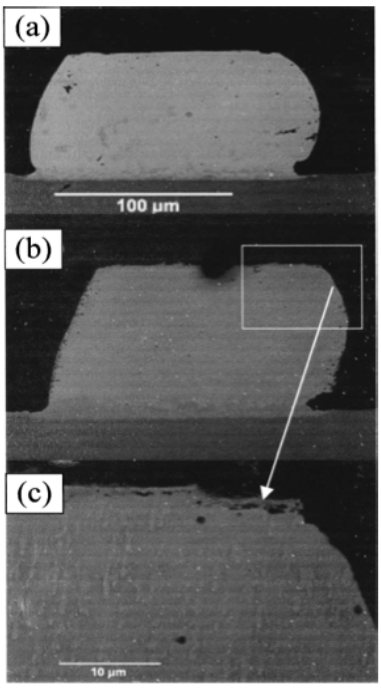
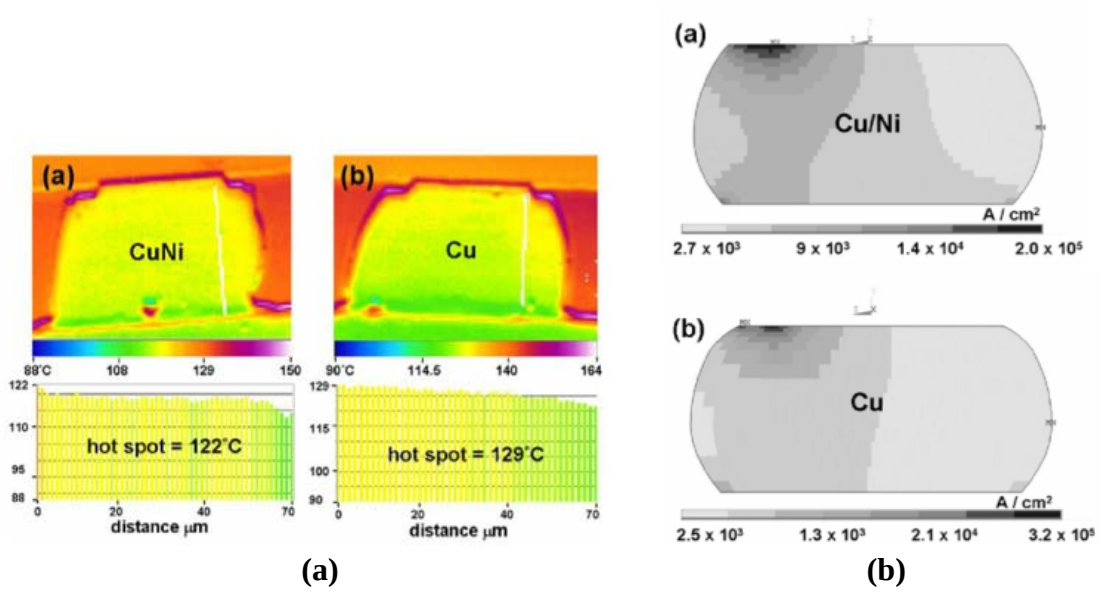


Figure 12. Void propagation sequence of a SnAgCu solder at 140°C and $3x10^4$ A/cm^2 at (a) 0 hours, (b) 14 hours, and (c) magnified image of (b) [22]

In 2008, H. Y. Chen et al. [23] experimented with 140µm diameter SAC solder and determined the effect of the UBM material on the bump's MTTF. Chen et al. experimented with Cu UBM as well as CuNi UBM. Considering Ni is a good barrier for Cu diffusion, the MTTF of the SAC solder with CuNi UBM was 27 times higher than the SAC solder with Cu UBM at $0.5x10^4$ A/cm^2 and 150°C. This result can be attributed to the peak current density of the Cu UBM system being $3.2x10^4$ A/cm^2 whereas the CuNi UBM system was only $2x10^4$ A/cm^2. Moreover, the joule heating was 7°C higher for the Cu UBM system versus the CuNi UBM system.



(a) **(b)**

Figure 13. (a) Temperature and (b) current distribution of CuNi UBM versus Cu UBM SAC solder [23]

Another study by W.C. Kuan et al. [24] explored the effect of bump size on the electromigration parameters of a SnAg solder bump. The bump diameter ranged from 200µm to 40µm as the entire bump system was evaluated at 100%, 80%, 60%, 40% and 20% of the original size. The experiment was done at a 100°C with a maximum applied current of 0.5A, equivalent to ~$1.5x10^3$ to $4x10^4$ A/cm^2 current density for the different bumps sizes. There was less current crowding observed when the bump diameter was decreased to 40µm. However, the joule heating effect showed an increase in bump

temperature that was 25.4 times greater at 40μm than at 200μm diameter. Joule heating at smaller bump sizes was a result of the increased temperature of the Al trace in addition to the increase in local and average current densities of the bump. In 2011, B. Vandevelde et al. [25] explored the MTTF for 90μm diameter SAC bumps with a maximum applied current density of $1.5x10^4$ A/cm^2 at 170°C. The highest lifetime, however, was shown for the SAC solder at 150°C and 0.7 $x10^4$ A/cm^2 where the sample survived for 574 hours.

1.3.3 Cu pillar with Solder Cap

The move towards Cu-based interconnections is because Cu has increased the electromigration lifetime of solder bump interconnections. With current crowding and joule heating playing a critical role in electromigration related failures, S.W. Liang et al. [26] used finite element modeling to see the effect of Cu UBM thickness on the current distribution of a solder bump. The flip chip bump that was modeled included 6 different layers: UBM layer, IMC layer, top layer of solder, middle layer of solder, necking layer of solder, and bottom layer of solder. The simulation was completed by applying 0.567A of current to an 184μm diameter solder bump and evaluating the peak current density at different UBM heights for each of the 6 layers. As previously mentioned, current crowding occurs at the entrance point of the bump during current stressing or what Liang et al. describes as the 'top layer of solder'. After increasing the UBM height from 5μm to 20μm, the current crowding ratio of the top layer of solder decreased from 8.7 to 1.5. The chart in Figure 14 shows the decrease in peak current density of the IMC layer and top layer of solder, the critical area where voids form, after increasing the UBM height. The solder bump with 20μm Cu UBM was concluded to have 33 times longer lifetime than the solder bump with 5μm Cu UBM.

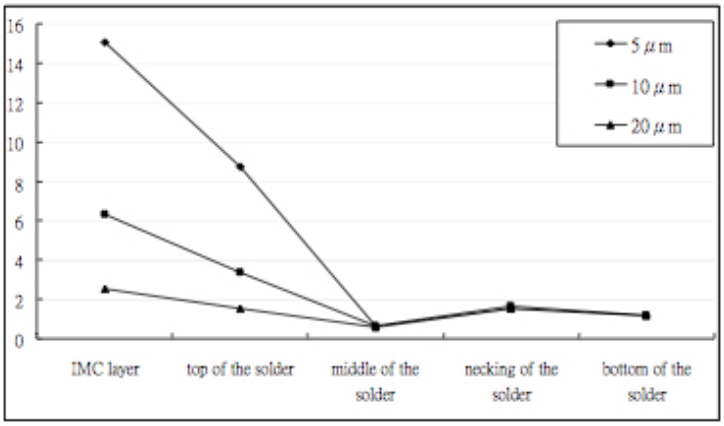


Figure 14. Crowding ratios for each layer of the solder joint for Cu thicknesses of 5µm, 10µm, and 20µm [26]

In a continuation of his research [27], S. W. Liang et al. examined the effect of UBM thickness on the amount of joule heating using finite element analysis. He concluded that by using a 100µm thick UBM, instead of 5µm, would decrease the overall hot spot temperature by 5°C. Though this was not a drastic change, the overall thermal gradient was significantly decreased from 400°C/cm to 60°C/cm. Liang et al. concluded that the minimal change in bump temperature was due to the Al trace (the primary heating source) not changing throughout the analysis. Also, Cu is a good heat conductor, meaning that it facilitates heat conduction despite its thickness. R. Labie et al. [28] in 2011 experimented with 80µm diameter Cu pillar with solder bumps, which were exposed to 300mA of current at 170°C. There was no resistance variation and only a 1°C change in temperature was observed for 1000 hours of testing. Moreover, there was no electromigration damage observed after cross-sectioning the sample. Another study by S. Lee et al. [29] from AdvanPack Solutions Pte Ltd was completed in 2005 using a test vehicle with 1600 Cu pillar with Sn bumps on a 10mm x 10mm die. The test vehicle was subjected to 1A of current at 150°C, equivalent to 1.27×10^4 A/cm^2 of current density. They noted that the die back temperature had reached 180°C due to joule heating. The failure mechanisms of the Cu pillar with solder bumps were investigated instead of MTTF. The regions that exhibited failure after 300 hours were the: 1) Cu pillar and Sn

interface and 2) substrate Cu pad to Sn interface. The first failure region was due to void initiation and propagation at the Cu-Sn IMC layer. Unlike regular solder bumps that witness UBM dissolution due to current crowding, the high current density in the Cu pillar caused rapid interstitial diffusion of Cu into Sn, forming a thick Cu-Sn IMC. The second failure region was due to the depletion of the IMC formed at the Cu pad to Sn interface as a result of flux divergence. In this case, the incoming flux of the Cu into the IMC was smaller than the outgoing flux, causing the IMC layer to shrink. After 300 hours of current stress, these failure regions can be seen in the following image.

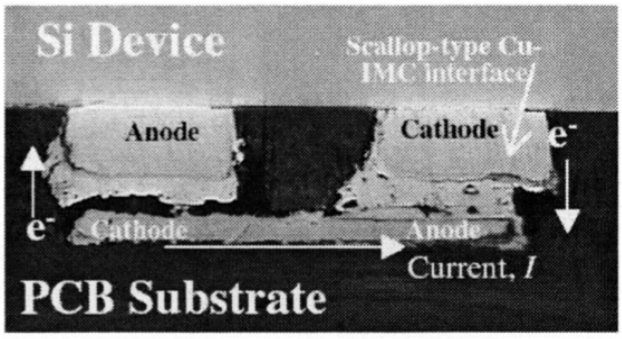


Figure 15. Cross-section showing electromigration failure of Cu pillar with Sn after 300 hours [29]

Lastly, a study by Y. Orii et al. [30] from IBM investigated the electromigration effects of their 80μm pitch Cu pillar bumps with solder, referred to as C2 flip chip interconnections. The testing conditions were $7x10^3$-$1x10^4$ A/cm^2 at 125°C-170°C. This experiment was different in that the samples were first put through an aging process for 2000 hours at 150°C. During current stressing at the mentioned temperatures, there were no failures recorded for 500 hours. Orii et al. concluded that the pre-aging process created thick IMC layers that acted as a barrier layer in preventing Cu from diffusing into the Sn solder, making the interconnection more electromigration resistant. The authors added finite element analysis and proved that the current density of the solder cap decreased as the Cu pillar height increased, as shown in Figure 16.

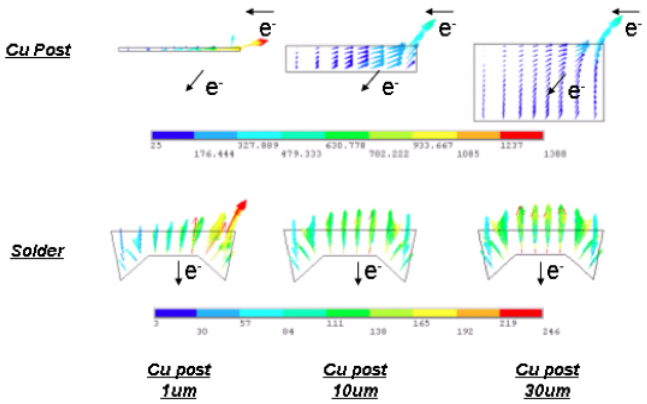
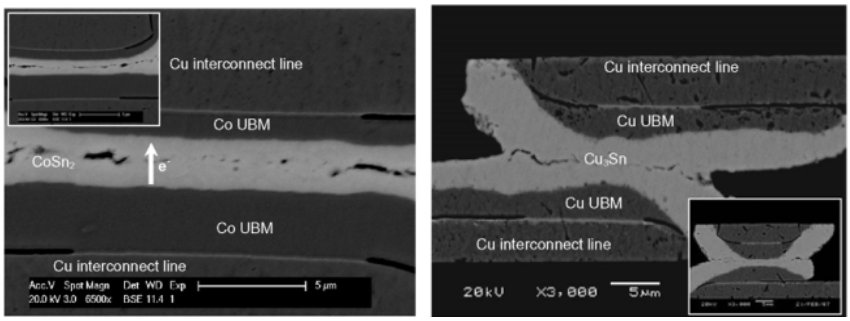


Figure 16. Current density distribution of the Cu and solder region for Cu pillar heights of 1µm, 10µm, 30µm [30]

1.3.4 Microbumps

Microbumps (µ-bumps) have been developed for advanced packaging technologies, such as 3D IC integration for high density applications. High density interconnections allow for increased signal bandwidth between multiple chipsets and also improved power distribution. S.L. Wright et al. [31] in 2006 studied the electromigration effects of 25µm bump structures using both CuSn and eutectic SnPb. Testing was performed on a chain of bump structures at 100°C- 155°C with stress currents of 62.5mA to 100mA, which is at a maximum current density of $3.2x10^4$ A/cm^2. The longest MTTF at the most extreme condition was around 6700 hours for the SnPb microbumps at 150°C and 100mA. The longest MTTF at the most extreme condition was more than 4000 hours for CuSn microbumps at 125°C and 100mA. The samples at higher temperatures failed because of thermal mechanisms. During failure analysis, it was determined that the SnPb bumps showed separation of Sn and Pb with Pb moving in the direction of electron flow. The CuSn bumps showed Sn interaction with the Ni barrier layers and also IMC formation on both sides of the bump. Failures occurred for the CuSn bumps near the top-surface-metal interface but were worse when electroless plating was used to deposit the Ni versus electrolytic.

In another study, R. Labie et al. [32] from IMEC experimented with purely intermetallic microbumps using Sn with Cu and cobalt (Co) at diameters of 20µm and 40µm. The testing was done for 1000 hours at 150°C with a current density of $6.3x10^4$ A/cm^2 without any failures. The bumps were initially deposited onto the die through electroplating. Then the silicon-to-silicon sample was bonded using a flip chip tool by applying a bonding temperature of 250°C with a maximum pressure of 67MPa. Once the electromigration testing was in process, there was no resistance change observed for the CoSn IMC joint. On the other hand, the CuSn IMC joint showed a decrease in resistance over time which eventually turned into a plateau. The microstructure evolution for both bumps was used to explain these results. The CoSn sample showed a single phase $CoSn_2$ intermetallic formation during bonding. However, the CuSn sample went through a phase transformation which included the initial two-phase state ($CuSn_3$ and Cu_6Sn_5) converting into a very stable, thermodynamically favorable single metallic phase of just $CuSn_3$.



(a) **(b)**

Figure 17. Cross-section of (a) Co-Sn IMC joint and (b) Cu-Sn IMC joint after 1000 hours at 150°C with 300mA of current stress [32]

C. C. Wei et al. [15] explored electromigration behaviors of CuSn microbumps as well. The bumps were stressed under 68°C to 164°C at current densities of $1.6x10^4$ A/cm^2 and $9.6x10^4$ A/cm^2. At maximum current and temperature stressing, the resistance of the microbumps steadily increased for 400 hours. Wei et al. mentioned that under certain stress conditions however, the resistance reached a plateau and no open failure was observed for a prolonged period of time. During failure analysis, it was concluded

that there was large IMC formation with minimum voids after current stressing. The IMC layer caused the steady increase in resistance due to its high resistivity. However, IMCs are known to be more electromigration resistant than Sn-based solder because of its high melting temperature. Electromigration induced failures are different in microbumps than C4 solder which, as previously mentioned, is dominated by void formation and UBM dissolution. Although there were no failures detected in the microbumps, it was declared that failures could occur by Cu consumption if disproportional amounts of solder volume and UBM thickness were selected.

In a thorough study [16] by Amkor in 2011, electromigration analysis of microbumps and Cu pillar bumps along with Pb-based and Pb-free solders was completed. The following table gives a comprehensive view of Amkor's electromigration analysis and is organized by the maximum current density applied at the highest oven temperature. It can be concluded that the microbumps, while providing the smallest dimension and therefore highest I/O density, is the most electromigration resistant interconnection technology. The factors affecting electromigration resistance was the amount of Sn available within the bump as well as the Cu thickness, either as substrate finish or UBM. Early failures occurred for the interconnections with a thick Cu finish but with low Sn content. An example of this was in the high Pb-solder where the Sn was completely depleted to form the Cu-Sn IMCs. On the other hand, the Cu pillars and microbumps with SnAg solder proved that the absence of Pb increased the electromigration resistance. However, the Cu thickness of these two interconnections was crucial, as a thicker Cu height had to be used to decrease the current crowding effect.

Table 2: Electromigration results from AMKOR at maximum current density [16]

Bump Type	Diameter	Max Current Density	Temperature	MTTF	Primary Failure Mechanism
Microbumps	25µm	3.5 x 10^4 A/cm^2	160°C	5500 hours	-No failures but asymmetric Cu consumption observed as well as possible Kirkendall voids
Cu pillar	90µm	~1 x 10^4 A/cm^2	145°C	8140 hours	-No EM related failures but asymmetric Cu consumption and cracks on substrate side observed
High Pb	75µm	~1.5 x 10^4 A/cm^2	145°C	799 hours	-Cracks between Cu-Sn IMCs and Cu substrate pad -Complete depletion of Sn to form CuSn IMCs
SnPb	75µm	~1.5 x 10^4 A/cm^2	145°C	742 hours	-Cracks on substrate side between the two Cu-Sn IMC phases -Cu consumption from the substrate pad -Some current crowding near UBM
SnAg	75µm	~1.5 x 10^4 A/cm^2	145°C	4180 hours	-Pan-cake type crack on UBM side -Cracking on substrate side

A summary of the electromigration analysis completed for all four interconnections in this section is listed in Tables 3-6. The tables do not include simulation data and only reflect experimental results and observed failure mechanisms.

Table 3: Electromigration analysis of Au stud bumps

Bump Type	Diameter	Max Current Density	Max Temperature	MTTF	Primary Failure Mechanism
Au Stud Bumps with ACA [18]	85µm	7×10^4 A/cm^2	N/A	12.28 hours	-Au-Al compounds to form due to joule heating -Al depletion because of electromigration -Crack formation between Au-Al compound and stud bumps -Adhesive delamination
Au Stud Bumps with Thermally Conductive ACA [19-20]	85µm	5×10^4 A/cm^2	N/A	200 hours	-Interface degradation between the non-solder bump and I/O pad metal due to IMC formation -Delamination and adhesive swelling due to joule heating

Table 4: Electromigration analysis of Pb-free solder bumps

Bump Type	Diameter	Max Current Density	Max Temperature	MTTF	Primary Failure Mechanism
Pb-Free Solder with Cu/Ni(V)/Al UBM [22]	125µm	2.25×10^4 A/cm^2	125°C	580 hours	-Current crowding -Joule heating -IMC dissolution
Pb-Free Solder with CuNi UBM [23]	140µm	0.58×10^4 A/cm^2	150°C	287 hours	-Void propagation through current crowding -Cu diffusion into solder
Pb-free Solder with NiAu UBM [25]	90µm	0.5×10^4 A/cm^2	170°C	188 hours	-Microstructural degradation through void formation at the interface of solder and IMCs

Table 5: Electromigration analysis of Cu pillar with solder bumps

Bump Type	Diameter	Max Current Density	Max Temperature	MTTF	Primary Failure Mechanism
Cu pillar with SnAg Solder [28]	80µm for both Cu and Solder	0.59 x 10^4 A/cm^2	170°C	1000 hours	-No failures
Cu pillar with Sn [29]	120µm for Cu and 140µm for Solder	1.27 x 10^4 A/cm^2	150°C	300 hours	-Void initiation and propagation at the Cu-Sn IMC layer - Depletion of the IMC formed at the Cu pad to solder interface due to flux divergence
Cu pillar with Solder after Aging Process [30]	40µm diameter for both Cu and Solder	1 x 10^4 A/cm^2	170°C	500 hours	-No failures

Table 6: Electromigration analysis of microbumps

Bump Type	Diameter	Max Current Density	Max Temperature	MTTF	Primary Failure Mechanism
Microbumps with various UBM barrier structures [31]	25µm PbSn bumps	3.2×10^4	150°C	6700 hours	-Separation of Sn and Pb with Pb movement in the direction of electron flow
	25µm SnCu bumps	3.2×10^4	125°C	>4000 hours	-Sn interaction with Ni barrier layers -IMC formation on both sides of bumps
Microbumps using Intermetallics (SnCo and CuCo) [32]	40µm	6.3×10^4 A/cm^2	150°C	1000 hours	-No failures: SnCo showed flat resistance and CuCo showed a decrease in resistance, which then reached a plateau
Cu with SnAg Microbumps [15]	40µm	9.6×10^4 A/cm^2	164°C	400 hours	-Increase in resistance over time due to IMC formation but no EM related voids

1.4 Limitations of Flip Chip Interconnections and Proposed Solution

The previous section establishes that electromigration testing has been done for existing interconnection technologies at a maximum current density of 10^4 A/cm^2. Therefore, Black's model can be used to predict the MTTF for these interconnections at higher current densities. J.R. Black, while formulating his model, made the claim that the MTTF was dependent on the square power of current density [7], where n= 2. As a result, if the current density was the only parameter increased by a factor of 10, for a specific interconnection, the MTTF would decrease by a factor of 100. This can be explained by Equation 8, shown below. $MTTF_1$ and J_1 represent the initial values, while $MTTF_2$ represent the mean-time-to-failure when J_2 is equivalent to $10(J_1)$.

$$MTTF_1 = AJ_1^{-2}\exp(\frac{E_A}{kT})$$
$$\Downarrow \qquad (8)$$
$$MTTF_2 = AJ_2^{-2}\exp(\frac{E_A}{kT}) = A\times\frac{1}{J_1*100}\exp(\frac{E_A}{kT})$$

This claim can be extended to the MTTF of Amkor's Cu pillar with solder interconnections in Table 2. If the current density applied was increased to 10^5 A/cm^2 for this case, then the MTTF would decrease to 81.4 hours, which is much less than the required operating lifetime of an electronic device.

The low current density threshold of flip chip solder bumps is the main limiting factor in achieving high electromigration resistance at smaller bump sizes. There are also concerns regarding Cu pillar with solder interconnections due to the formation of IMC layers. Failures have been reported showing void initiation and propagation at the Cu-Sn IMC layer as well as IMC depletion at the Cu pad and solder interface [29]. Moreover, although gold stud bumping can be used to achieve finer pitch, the high cost of bumps along with the low current carrying capability of ACF/ACAs limits its adoption in the packaging industry [33]. Therefore, a new low-cost, ultra-fine pitch interconnection

technique needs to be explored and evaluated at higher current densities to overcome and surpass existing flip chip interconnection methods.

1.4.1 GT-PRC Cu-Cu Interconnections

As part of the SOP vision, GT-PRC introduced an advanced flip chip technique which involves chip-last embedding with low-cost and low temperature Cu-Cu interconnections to achieve higher I/O density. Chip embedding has several advantages which include decrease in package size, high electrical performance due to short and well-controlled interconnects, and good reliability due to a homogenous mechanical environment surrounding the embedded chips [34]. Consequently, the chip-last approach was developed by GT-PRC, which exceeds existing embedding technologies by providing better yield, higher reliability, ease of re-workability, and better thermal management. The approach involves assembling the chips in the last step of module fabrication. Initially, a cavity within the build-up layer of the substrate is fabricated and then the active die is embedded with appropriate electrical interconnections [35].

The Cu-Cu interconnection technique utilized in the chip-last approach is a potential candidate for the next generation of flip chip interconnections. It has been demonstrated at 30µm pitch and less than 20µm stand-off height. The dies are bonded using a non-conductive film (NCF) and assembled using thermo-compression bonding at 180°C.

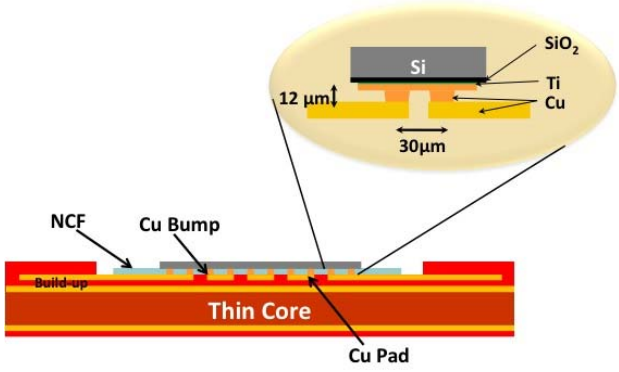
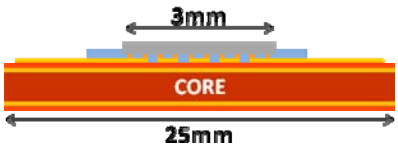
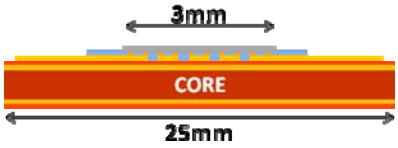
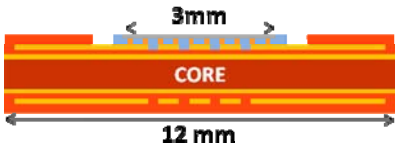
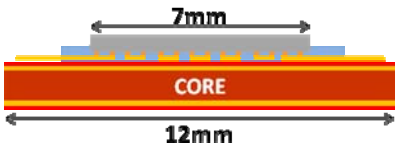


Figure 18. Schematic of chip-last embedded Cu-Cu interconnections [36]

To test the versatility of this interconnection architecture, different die sizes and thicknesses were implemented and assembled on the surface of the substrate as well as within cavities. Reliability analysis was completed under High Temperature Storage Life Test (HTS), Unbiased Highly Accelerated Stress Test (U-HAST), and Thermal Cycling Test (TCT) with results establishing high thermo-mechanical reliability for each different test vehicle, as shown in Table 7 [36].

Table 7: Reliability analysis of each chip-last test vehicle [36]

Test Vehicle	Description	Reliability Analysis
	• 550µm thick die • 360 bumps • 30µm pitch • Surface assembly	HTS [175°C in air for 72 hours]: Survived 72 hours with only a ~3% increase in resistance
		U-HAST [130°C / 85%RH for 96 hours]: No moisture ingress or delamination after 192 hours
		TCT [55°C to 125°C]: >2000 cycles without failure
	• 550µm thick die • 360 bumps • 30µm pitch • Surface assembly	TCT [55°C to 125°C]: >1000 cycles without failure
	• 55µm thick die • 261 bumps • 50µm pitch • Cavity assembly	TCT [55°C to 125°C]: ~1000 cycles without failure
	• 550µm thick die • 537 bumps • 50µm pitch • Surface assembly	TCT [55°C to 125°C]: 500 cycles without failure

1.5 Thesis Objective

The objective of this thesis is to analyze and understand the adhesive-based Cu-Cu interconnection technique under extreme current and temperature conditions. In order to examine the electromigration resistance of this new interconnection scheme, a test vehicle was fabricated reflecting the future needs of the semiconductor industry in terms of finer pitch and higher pin-count. The test vehicle included a 5mm x 5mm die with 30μm diameter Cu-Cu interconnections arranged in an area-array format with a minimum bump pitch of 100μm. The Cu-Cu interconnections were created through thermo-compression bonding at 180°C. This interconnection technique has two major technical challenges, which includes obtaining high electromigration resistance at 1) small diameter and 2) with a low temperature bonding method. At a low bonding temperature of 180°C, a mechanical bond is created instead of a metallurgical bond, which has never been explored under high current density.

In order to achieve the goal of this research, finite-element analysis was conducted to investigate the current crowding and joule heating effects of the Cu-Cu interconnection along with two existing bump technologies, Cu pillar with solder and Pb-free solder. Experimental testing was also completed to validate the thermo-mechanical reliability and investigate the current carrying capability of the Cu-Cu interconnections. This interconnection technology was based on the chip-last approach, which has already been proven to be highly reliable under various conditions. The present work aims to understand the basic mechanisms behind this superior reliability and demonstrate how flip chip packaging can be extended beyond solders for smaller pitch and higher current densities.

1.6 Thesis Outline

This research confirms the high thermo-mechanical reliability and investigates the electromigration reliability of 30μm diameter Cu-Cu interconnections without solder.

Chapter 2 begins with the design parameters used to construct the 3D models in ANSYS of the Cu-Cu, Cu pillar with solder cap, and Pb-free solder bump interconnections. The current crowding and joule heating effects are subsequently evaluated for all three bump structures. A final conclusion is made regarding why an all-copper system is better than solder-based interconnections.

Chapter 3 discusses design and fabrication of the area-array test vehicle. The process flow used for fabrication is stated for both the die and substrate. The conditions employed for low temperature Cu-Cu thermo-compression bonding are also stated. Finally, the chapter ends with the testing method used for electromigration analysis of the Cu-Cu interconnections.

Chapter 4 states the observations made with C-SAM and cross-sectioning before and after subjecting the area-array assemblies to thermal cycling. The results obtained after TCT is disclosed to prove the high thermo-mechanical reliability of the Cu-Cu interconnections. Next, electromigration testing results at 10^4 A/cm^2 to 10^6 A/cm^2 and 130°C are discussed and a conclusion is made regarding the Cu-Cu interconnections under high current and temperature stress.

In conclusion, Chapter 5 highlights the main results obtained in each chapter. It also provides suggestions for future work in order to advance the Cu-Cu interconnection technology.

CHAPTER 2

FINITE ELEMENT MODELING OF THREE FLIP CHIP BUMP STRUCTURES

This chapter discusses the joule heating and current crowding effects of the Cu-Cu interconnection in comparison with two existing flip chip interconnections, Cu pillar with solder (CuSn) and Pb-free solder, using Finite Element Modeling (FEM). The Cu-Cu interconnection represents the all-copper system fabricated at GT-PRC and the objective was to compare this bump architecture to the state-of-the-art Cu pillar with solder cap found in the industry today as well as the more common solder bump used in most flip chip packages.

2.1 Design Parameters for Bump Structures

Black's model [11] uses current density and temperature to analyze the electromigration resistance of an interconnection. However, this equation does not take into account the current crowding and joule heating effects caused by electromigration. Accordingly, K. N. Tu et al. proposed [11] a modification of Black's model to include these two factors so as to properly estimate the MTTF:

$$MTTF = A(c \cdot J^{-n}) \exp\left(\frac{E_A}{k(T + \Delta T)}\right) \qquad (9)$$

In this equation, c is the current crowding factor and ΔT is the temperature increase due to joule heating.

To understand the effects of these two parameters, rudimentary 3D models were constructed with ANSYS. Three distinctive packages were created, as shown in Figure 19. The components of the package included a silicon die, Bismaleimide Triazine (BT)

substrate, and NCF surrounding a single interconnection. Three different types of interconnections were constructed within each package, as depicted in Figures 20-22.

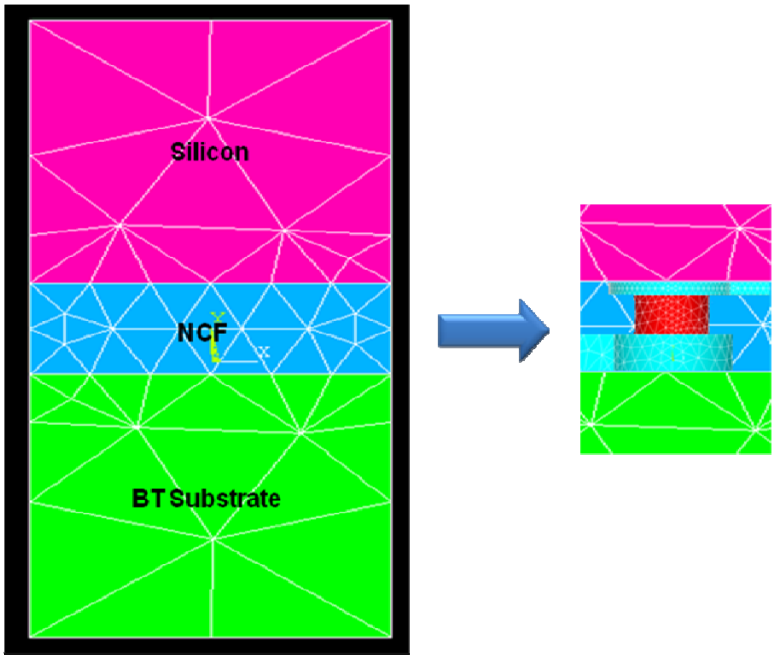


Figure 19. ANSYS model of the entire package, which includes a silicon die, BT substrate, and NCF surrounding a single interconnection

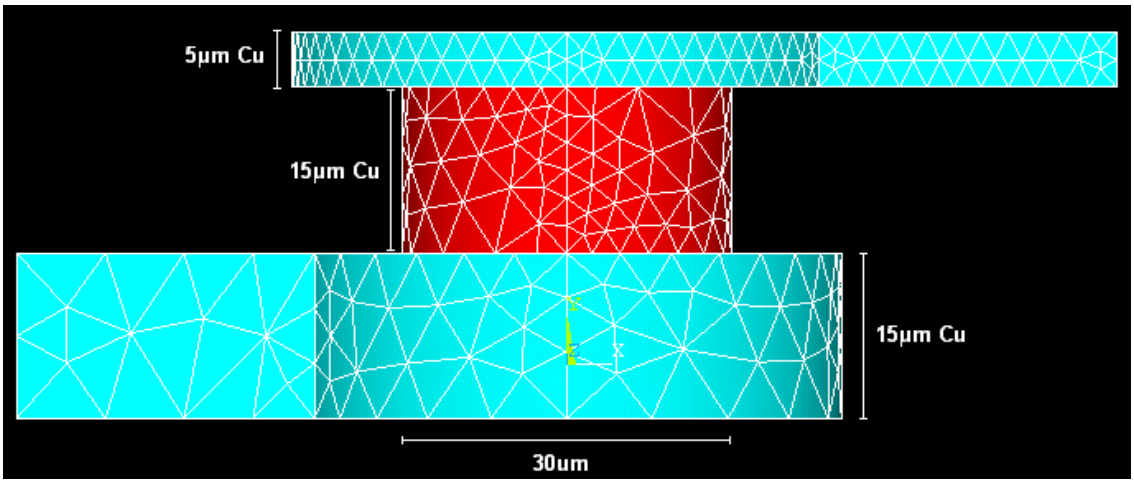


Figure 20. ANSYS model of Cu-Cu interconnection

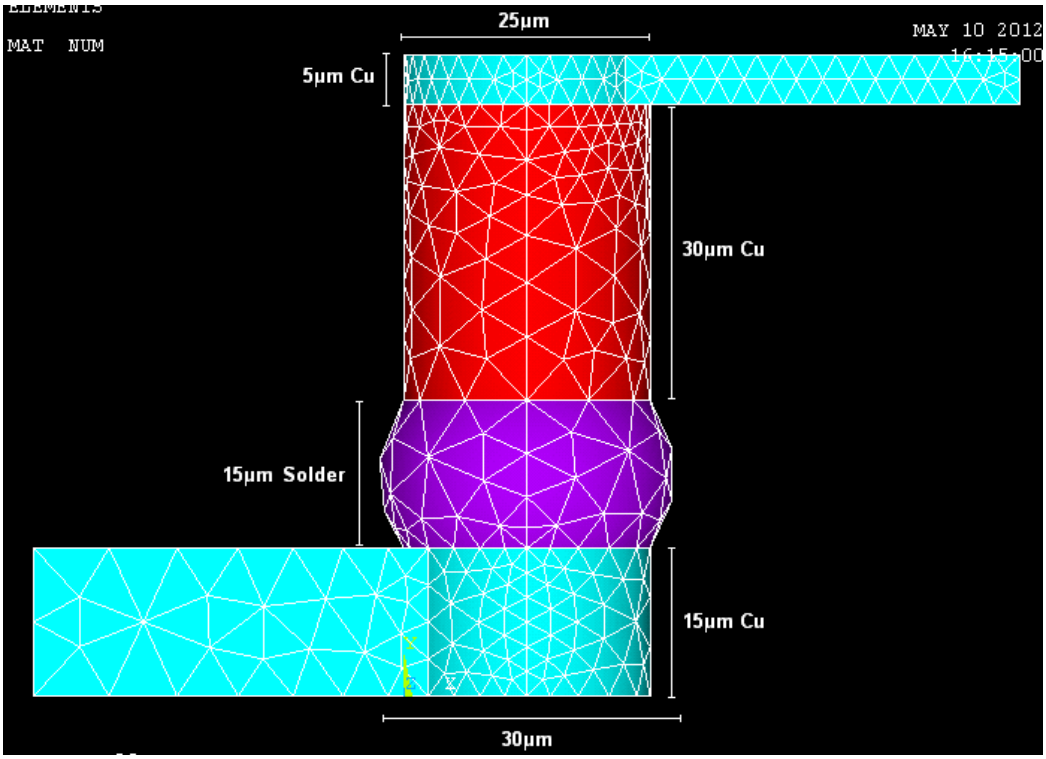


Figure 21. ANSYS model of Cu pillar with solder cap

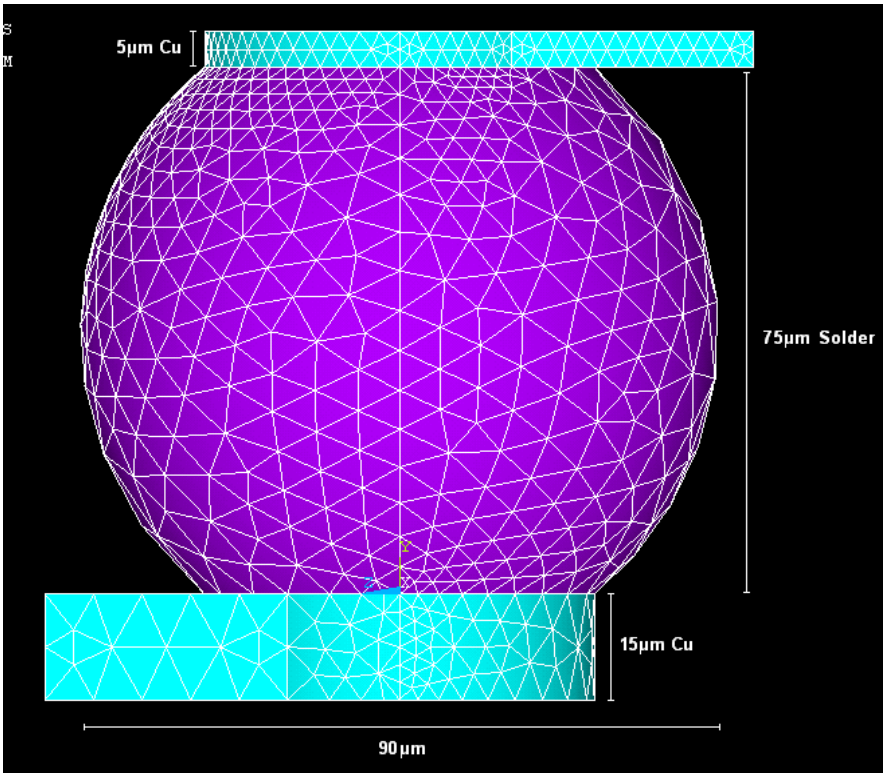
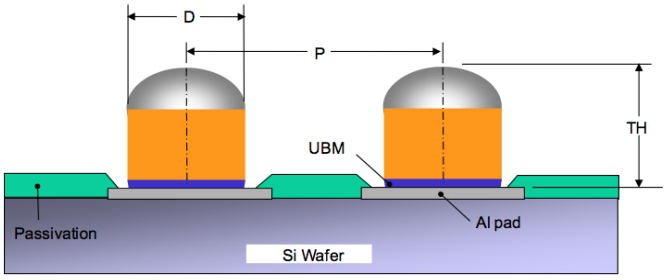


Figure 22. ANSYS model of Pb-free solder bump

The element type used was SOLID 226 given its suitability for thermal-electric coupled analysis. There were many control parameters employed in the model in order to keep consistency among all three structures. The dimensions and material properties for the silicon die and substrate were kept the same. The material property for NCF was also kept the same but the height differed according to the total bump height added to the top trace and bottom pad thicknesses. The material and thickness of the trace and pad were kept identical as to not influence the joule heating and current crowding effects.

The 3D model of the Cu-Cu interconnection closely resembled the actual test vehicle discussed in the next chapter. It was modeled with 15µm height and 30µm diameter. The CuSn interconnection dimensions were taken from the industry's first ultra-fine pitch Cu pillar with solder flip chip [37], shown in Figure 23. The bump modeled in ANSYS included a Cu pillar with a height of 30µm and diameter of 25µm in addition to a solder cap with a height of 15µm and diameter of 30µm. The lower cost and 50µm fine pitch capabilities of this interconnection makes it ideal for high density applications. As mentioned in Chapter 1, this interconnection technique had a MTTF of more than 8000 hours at 145°C and 10^4 A/cm^2 applied current density [16].



Feature	Dimension
Pitch (P)	50 - 100um
Cu Pillar diameter (D)	20 - 50um
Total height (TH)	30 - 45um

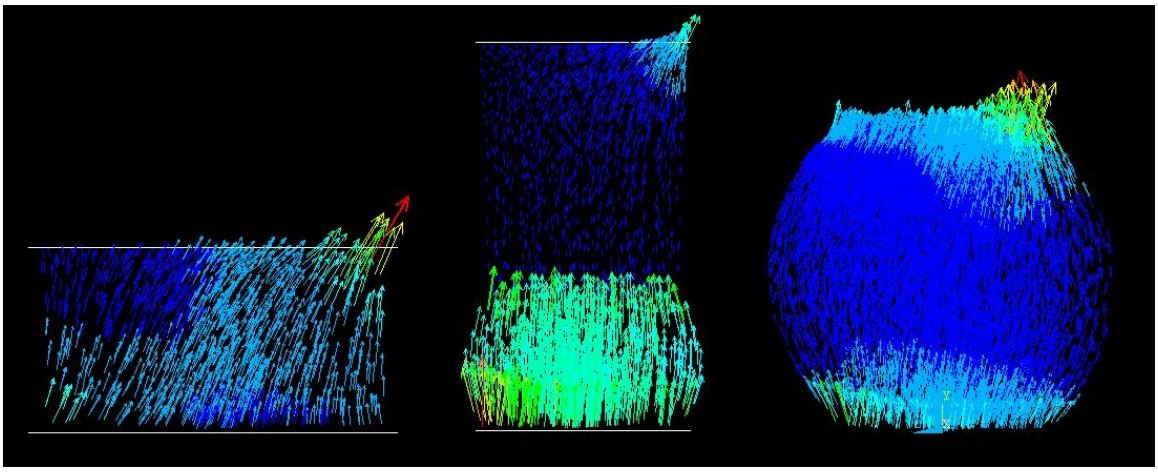
Figure 23. Cu pillar with solder interconnection dimensions [37]

The Pb-free solder bump was modeled after current bumping capabilities at 90µm diameter and 75µm height [38]. This current flip chip technology has been limited to 180µm pitch due to electromigration concerns at smaller bump dimensions.

The parameters used to define each material included electrical resistivity, thermal conductivity, specific heat, and mass density, which are listed in Table 8. Once the bump geometry was created, it was free meshed into tetrahedral shapes. A current of 1A was passed through the bottom Cu pad while the top Cu trace was grounded at 0V. The vector plots of the electric field for each interconnection is shown in Figure 24.

Table 8: Material properties used in ANSYS

Material	Electrical Resistivity (ohm-cm)	Thermal Conductivity (W/cm-K)	Specific Heat (J/gram-K)	Mass Density (g/cm^3)
Cu	1.68×10^{-6}	4.01	0.386	8.94
Solder (SAC305)	13.2×10^{-6}	0.587	0.232	7.39
Silicon Die	2.35×10^{5}	1.3	0.7	22.33
BT Substrate	1×10^{16}	0.0037	0.8	1.8
NCF	1×10^{13}	0.002	1.11	1.23



(a) **(b)** **(c)**

Figure 24. Vector plots of the electric field for an input current of 1A for the a) Cu-Cu b) Cu pillar with solder and c) Pb-free solder interconnection

Appropriate temperature boundary conditions were applied to evaluate the temperature across each bump under current stress. For a flip chip without an exposed

heat spreader or heat sink, 80-90% of the heat typically flows towards the substrates side and through the BGAs [39]. Therefore, a uniform temperature of 298K was set to the bottom of the substrate while adiabatic boundary conditions were set to the four sides of the package as well as the top. The four factors investigated in ANSYS were the peak current density, current crowding ratio, joule heating, and peak bump temperature.

2.2 Current Crowding and Joule Heating Results

2.2.1 Current Crowding Effect

2.2.1.1 Peak Current Density

The results from ANSYS were used to analyze the current crowding effect which induces electromigration failures in flip chip interconnections [10]. The applied current of 1A was equivalent to an average current density of 10^5 A/cm^2 for both the Cu-Cu and CuSn interconnections, but only 10^4 A/cm^2 for the solder bump. However, as previously discussed, the line-to-bump configuration creates a sharp change in current density, which results in current crowding or non-uniform distribution of current through the bump. Consequently, a peak current density, which is higher than the expected average current density, is observed at the entrance of the bump where electrons enter the interconnection from the Cu trace. Therefore, the first step was determining the peak current density within each bump through ANSYS. The results are shown in Table 9 in the order of highest to lowest peak current density.

Table 9: Peak current densities of bumps

Interconnection	Current Density (A/cm^2)
CuSn	1.63×10^6
Cu-Cu	6.97×10^5
Solder bump	1.06×10^5

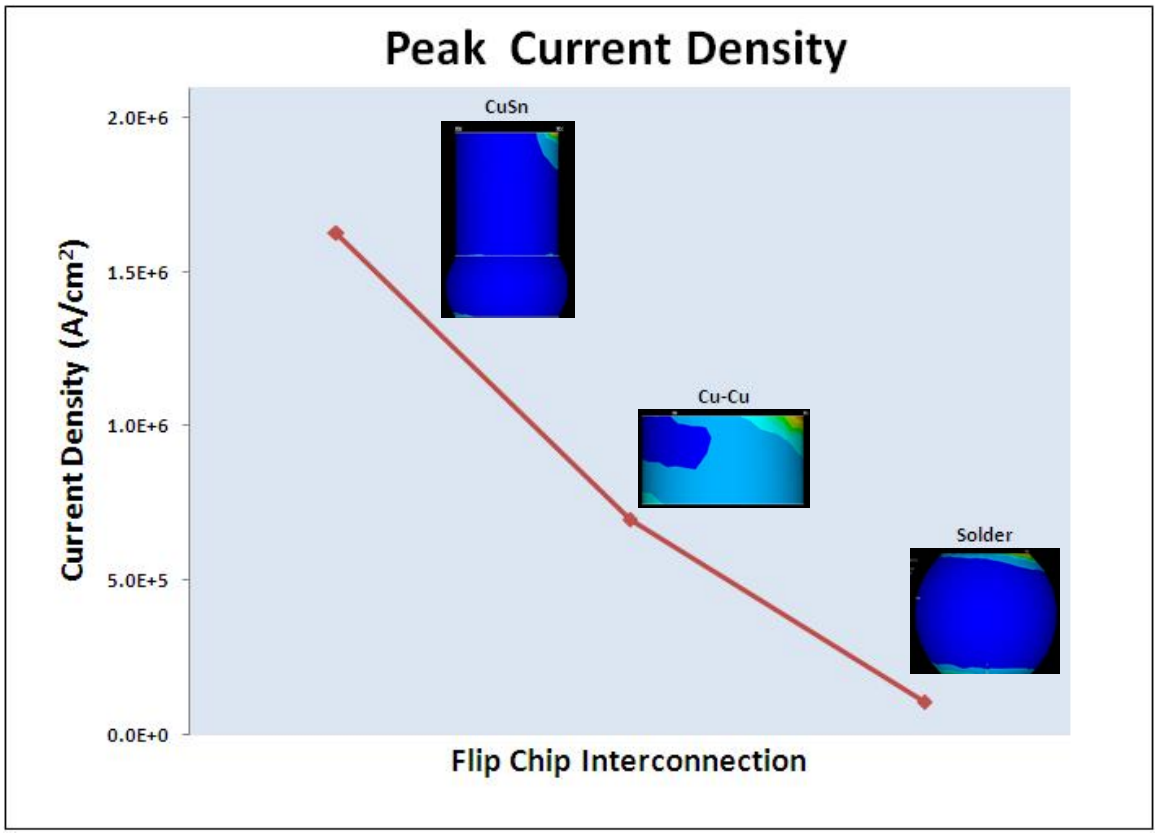


Figure 25. Plot showing peak current density of each bump

To understand the reasoning behind these results, the equation for current density can be recalled in Equation 10, in which current density is inversely proportional to resistivity.

$$J = \sigma E \rightarrow J = \frac{1}{\rho} E \quad (10)$$

Given the resistivity values in Table 8, Cu has lower resistivity than solder. Thus, the two Cu-based interconnections have a higher peak current density. Further dissecting Equation 10 establishes that length is directly proportional to current density.

$$J = \frac{1}{\rho} E \rightarrow J = \frac{1}{R} \frac{l}{A} E \quad (11)$$

The CuSn interconnection therefore, exhibits the highest peak current density due to its greater length. However, the Cu pillar assists in alleviating the non-uniform distribution

of current density from the top Cu trace to the solder because of its geometry and lower resistivity, as shown in Figure 26 [29].

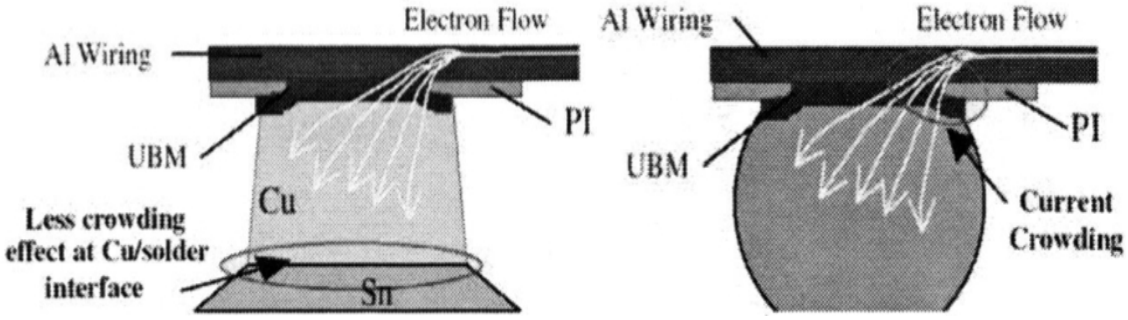


Figure 26. Current crowding effect in (a) Cu pillar bump with solder and (b) solder bump [29]

2.2.1.2 Current Crowding Ratio

After the peak current density, the next step was evaluating the current crowding ratio. The ratio was determined by taking the peak current density in the bumps divided by the average current density in the UBM opening [40], as shown in Equation 12. The results are shown in Table 10 from highest to lowest current crowding ratio.

$$C.C.R = \frac{J_{\max,bump}}{J_{average,UBM\_opening}} = \frac{J_{\max,bump}}{I \Big/ \pi r^2_{UBM\ opening}} \quad (12)$$

The interconnections with high peak current density and large UBM opening cross-sectional area had a larger current crowding ratio. As a result, the CuSn had the highest current crowding ratio, while the solder bump had the lowest.

Table 10: Current crowding ratios of bumps

Interconnection	Current Crowding Ratio
CuSn	8.00
Cu-Cu	4.93
Solder bump	2.52

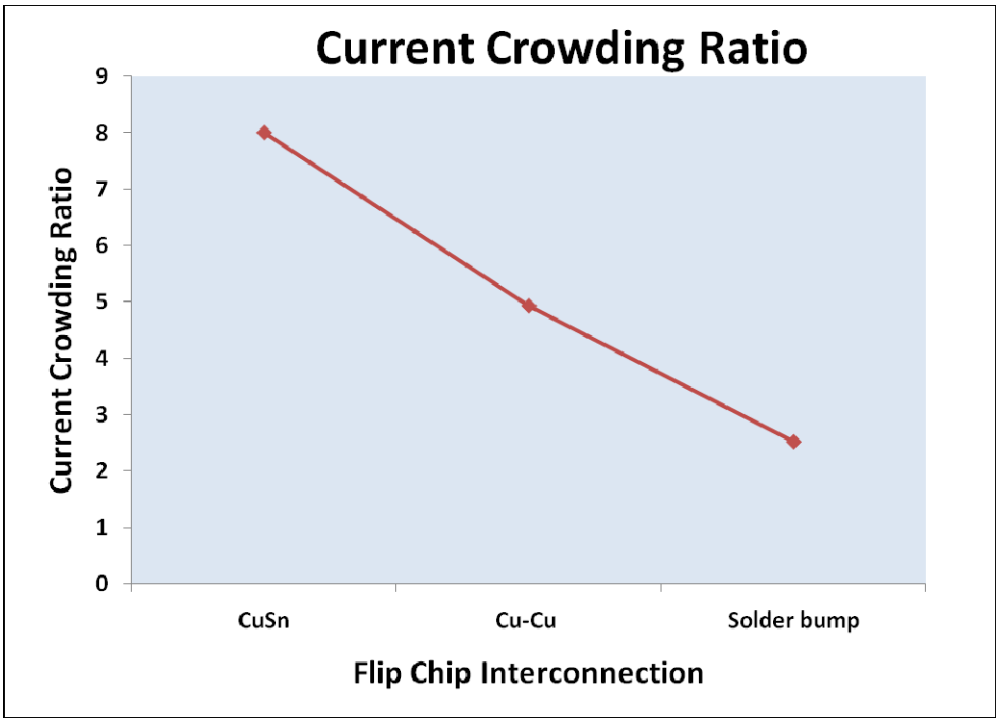


Figure 27. Plot showing the current crowding ratio of each bump

2.2.2 Joule Heating Effect

2.2.2.1 Joule Heat Generation

The ability to perform thermo-electric coupled analysis in ANSYS, allowed for joule heat generation to be attained. The following table provides the maximum joule heating values of each interconnection. The trend of these results can be predicted by Equation 7 in Chapter 1.

Table 11: Joule heat generation of bumps

Interconnection	Joule Heat Generation ($J/s \cdot cm^3$)
CuSn	1.84×10^6
Cu-Cu	3.52×10^5
Solder bump	9.73×10^4

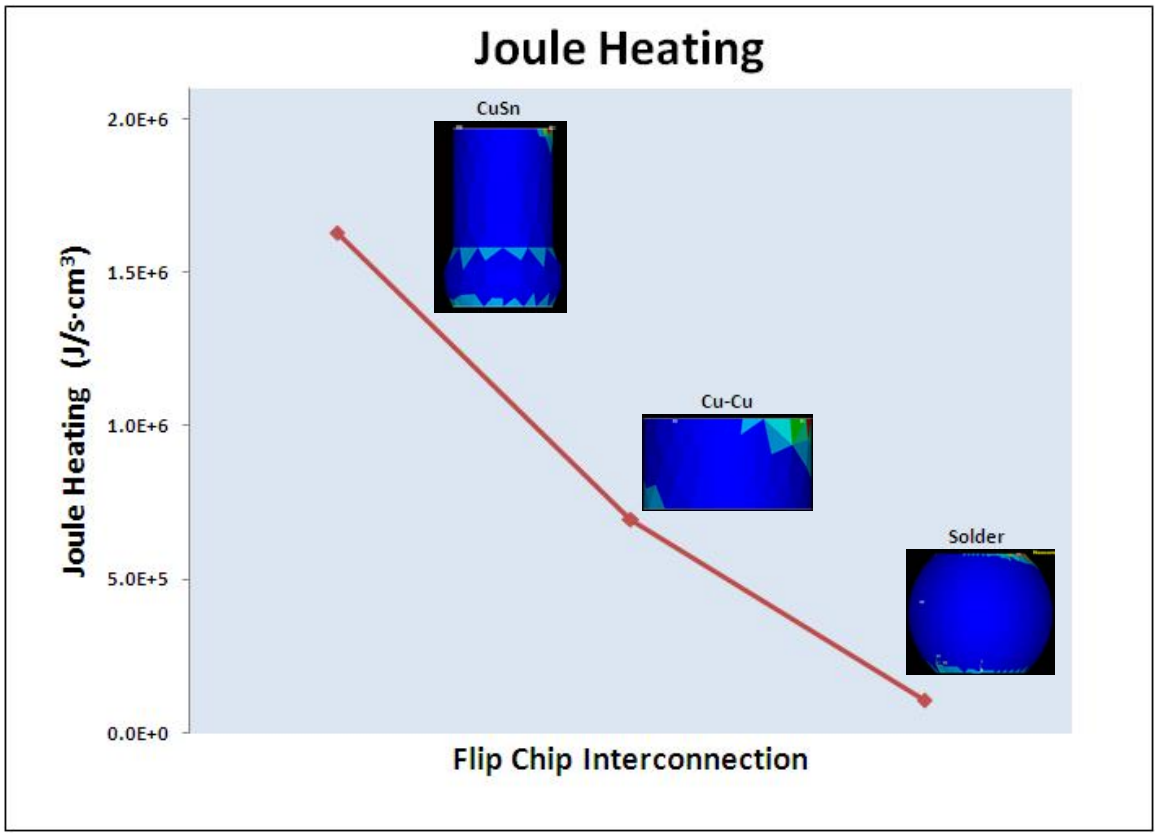


Figure 28. Plot showing the amount of joule heating in each bump

K. N. Tu et al. stated that the joule heating rate can be approximated by multiplying the squared average current density of each bump by its resistivity [12]. The average current density was evaluated by dividing the 1A of applied current by the cross-sectional area of each structure. The estimated joule heating rate, from highest to lowest, was calculated to be: 6.97 x 10^4 J/s·cm^3 for the CuSn interconnection, 3.36 x 10^4 J/s·cm^3 for the Cu-Cu interconnection and 3.26 x 10^3 J/s·cm^3 for the solder bump. These calculations are consistent with the ANSYS results.

2.2.2.2 Maximum Bump Temperature

The last analysis was determining the temperature distribution across each bump with a current input of 1A. The maximum temperature was also expected to be located at the top right corner where the electrons flows from the Cu trace to the bump, causing current crowding and thus joule heating. The maximum temperature of each bump is

listed in Table 12 and the results follow a similar trend seen for joule heating. The bumps with high joule heating also had a high bump temperature.

Table 12: Maximum temperature of bumps

Interconnection	Max Bump Temperature (K)
CuSn	543.338
Cu-Cu	380.134
Solder bump	328.171

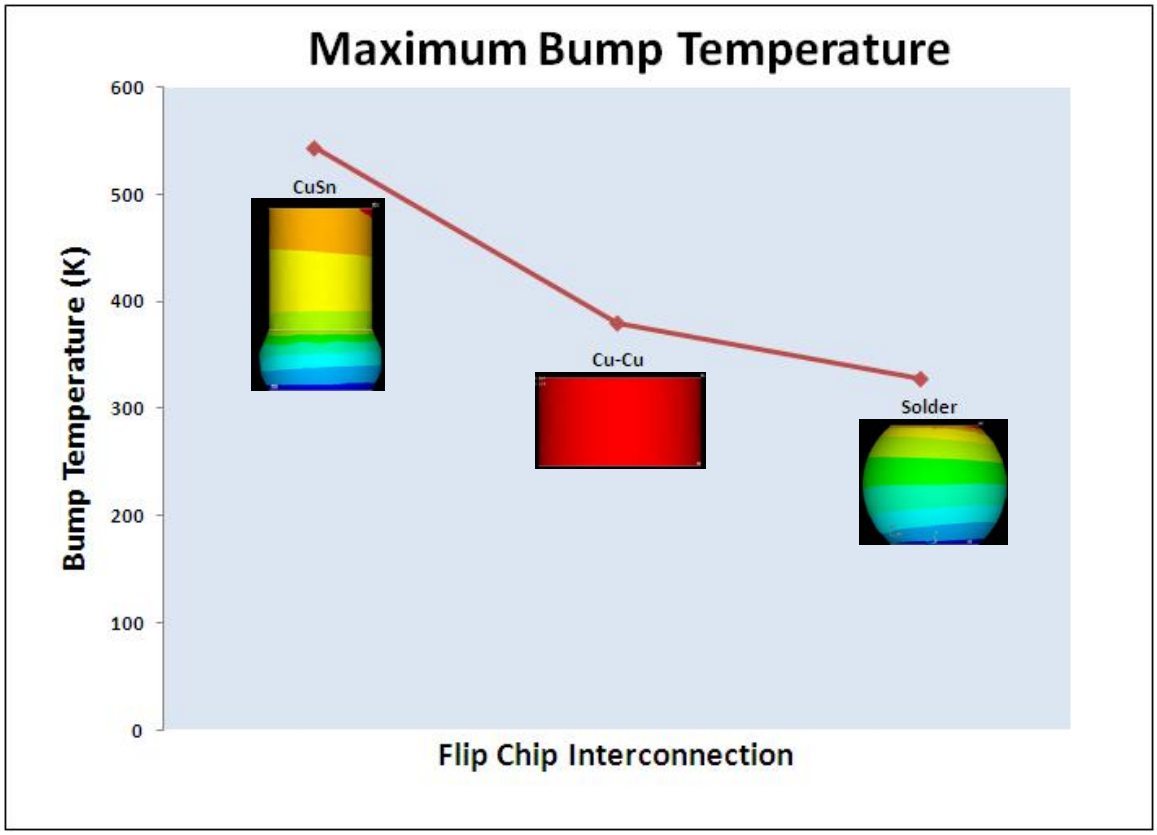


Figure 29. Plot showing maximum temperature of each bump

In this investigation, thermal conductivity influenced how well the temperature, due to joule heating, was dissipated across each bump. Cu has approximately eight times higher thermal conductivity than solder. However, the CuSn interconnection had the highest bump temperature because of its high peak current density. Furthermore, the solder bump had the lowest temperature, despite its low thermal conductivity, because of

its large cross-sectional area. The Cu-Cu interconnection did not show the lowest bump temperature, but it witnessed a negligible temperature gradient across the bump. The Cu-Cu interconnection effectively dissipated the heat generated by joule heating.

2.3 Solder Pillar vs. Cu-Cu

Difference in bump geometry and structures can directly affect electromigration performance because of current crowding. JEDEC standards for characterizing electromigration states that the bump height, bump diameter, UBM composition, UBM thickness, and semiconductor die metallization influence the outcome of an interconnection's electromigration performance [41]. To address the effect of the bump material on current crowding and joule heating, free of influence from the geometry or bump structure, another investigation was completed with ANSYS.

An identical Cu-Cu interconnection structure was analyzed while varying only the material of the bump from Cu to solder. The peak current density, current crowding ratio, joule heating, and maximum bump temperature was once again repeated for this new interconnection.

Table 13: Values for solder pillar structure compared to the Cu-Cu interconnection

Parameters	Solder Pillar	Cu-Cu
Peak Current Density	2.11×10^5	6.97×10^5
Current Crowding Ratio	1.49	4.93
Joule Heat Generation	3.62×10^5	3.52×10^5
Max Bump Temperature	421.535	380.134

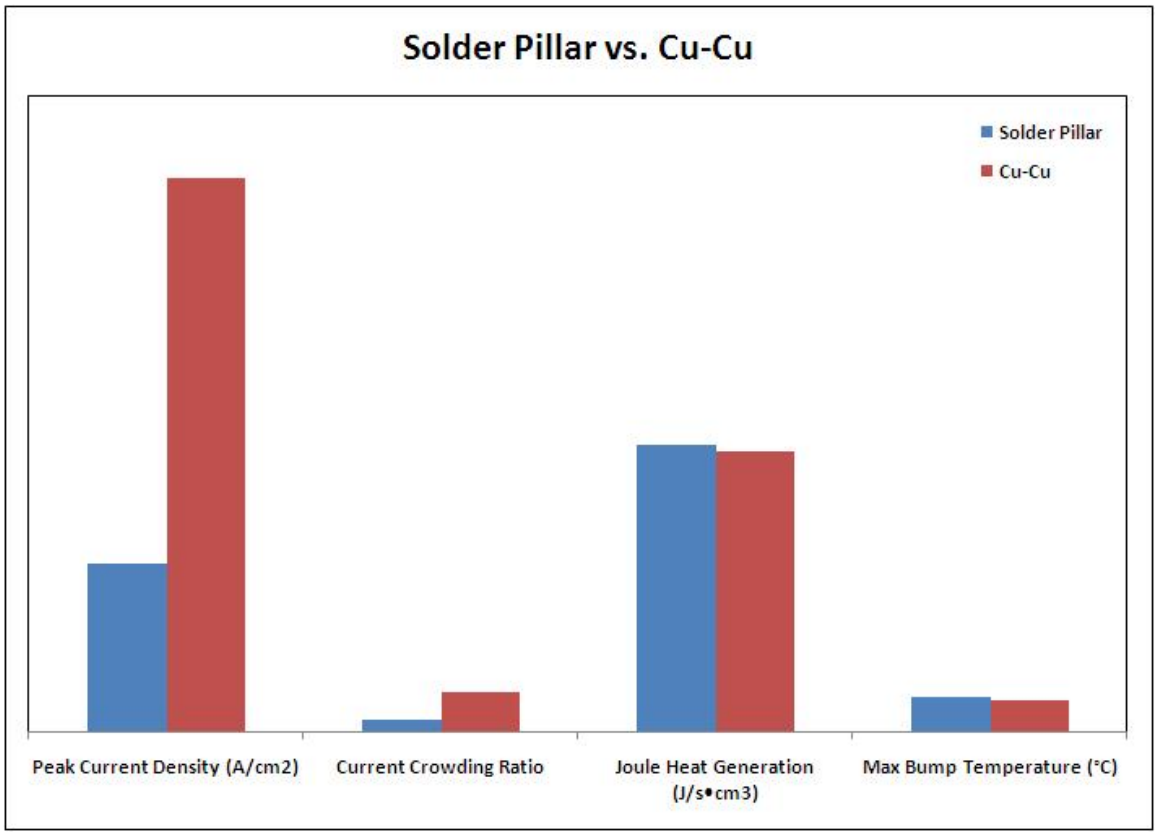
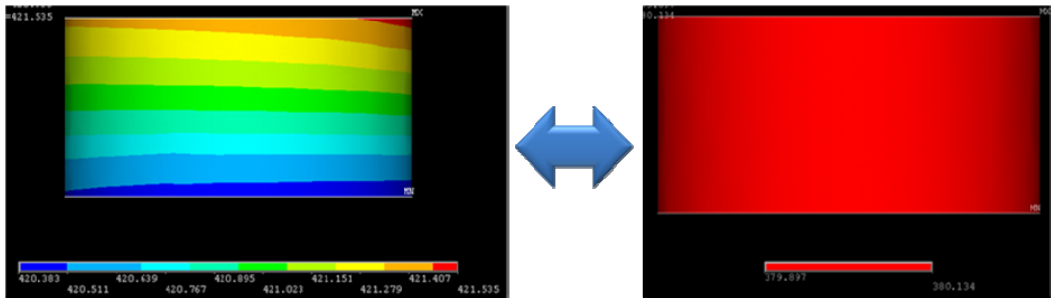


Figure 30. Plot showing each parameter for both the solder pillar and Cu-Cu interconnection

As shown in Table 13, the solder pillar had lower peak current density and a smaller current crowding ratio than the Cu-Cu interconnection due to its higher resistivity. However, it experienced more joule heating and had a higher bump temperature. Also, the heat generated, due to joule heating ,was not distributed uniformly across the bump like the Cu-Cu interconnection, as seen in Figure 31.



(a) **(b)**

Figure 31. Temperature distribution of the a) solder pillar interconnection and b) the Cu-Cu interconnection

As previously mentioned, joule heating is proportional to the square of the current density. This implies that although the Cu-Cu interconnection experiences high current density, it is capable of dissipating the heat generated by these high currents. The Cu-Cu interconnection's ability to maintain a uniform bump temperature at 1A of current stress suggests less chance of flux divergence and therefore, a lower probability of failure.

The Cu-Cu interconnection at 30μm diameter proves to be most resistant towards current crowding and joule heating. The CuSn interconnection had the highest peak current density, current crowding ratio, joule heating, and bump temperature. Though the solder bump had the lowest value for all four parameters investigated, its volume was significantly larger. The applied current of 1A was equivalent to 10^4 A/cm^2 of current density for the solder bump. In order to match the average current density of the Cu-Cu interconnection at 10^5 A/cm^2, a current of 6.36A would need to be applied. The flip chip solder bump at 90μm diameter is merely a control sample for which electromigration is not yet a severe concern.

2.4 Why is Cu Better than Solder?

In addition to the ANSYS results, Cu is more advantageous than solder-based interconnections due to its superior electrical and thermal characteristics. Cu has a higher melting point (1356 K) [7] than SAC solder (490.15 K) [42], resulting in a slower diffusion rate. The low melting point of SAC solder increases the chance of void and hillock formation due to electromigration. From the phenomenological equation of atomic flux, K. N. Tu in 1997 [7] derived an equation to evaluate the threshold for electromigration. His equation defined the "critical product", which is dependent on the Young's modulus, *Y*, resistivity, ρ, and effective charge number, *Z*e*, of the interconnect material:

$$j\Delta x = \frac{\mathrm{Y}\Delta\varepsilon\Omega}{Z^* e\rho} \quad (13)$$

K. N. Tu stated that interconnections designed with a product of $j\Delta x$ less than the critical product would exhibit no electromigration failure [7]. Consequently, it can be proven from Equation 13 that the current density required to cause electromigration is two orders of magnitude smaller in SAC solder than in Cu, if Δx is kept constant. Table 14 confirms that the SAC solder has a Young's modulus which is half that of Cu, and has one magnitude higher resistivity and effective charge. Given that electromigration occurs in solder at approximately 10^4 A/cm^2, it can be concluded that Cu can handle current densities up to 10^6 A/cm^2.

Table 14: Critical product parameters for Cu and SAC solder

Parameter	Cu [11,43,44]	SAC solder [45-47]
Young's Modulus (GPa)	110	47.9 - 51
Resistivity (ohm-cm)	1.68×10^{-6}	1.32×10^{-5}
Effective Charge	5.8	20

Another factor that affects electromigration is flux divergence, which occurs due to variance in microstructure, material type, and temperature. With solder bumps, there are many different materials that make up the bump structure. The UBM itself has many components, including an adhesion layer, barrier layer, wetting layer, and anti-oxidation layer, each of which are made up of different materials. Due to the varying diffusivity and resistivity found among these different materials, flux divergence occurs at the interface between them. For example, atoms diffuse much faster in solder than in the UBM, thus causing void formation at their interface [48].

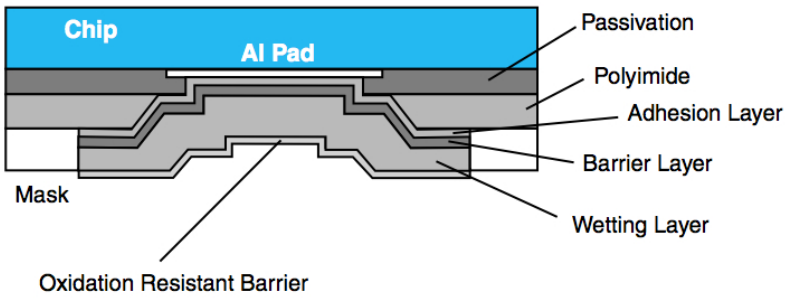


Figure 32. UBM layers of a flip chip solder bump [4]

The structure of the proposed Cu-Cu interconnection however, is far simpler. The bump starts with a Cu pad layer, equivalent to a redistribution layer, which connects to a Cu pillar structure and then to the Cu substrate pad. To minimize oxidation of Cu, a surface finish made up of Ni, Pd, and Au exists on both sides of the Cu pillar and Cu substrate pad, a potential area for failures. However, the thin amount of surface finish suggests that it will not be a major factor in causing electromigration failures.

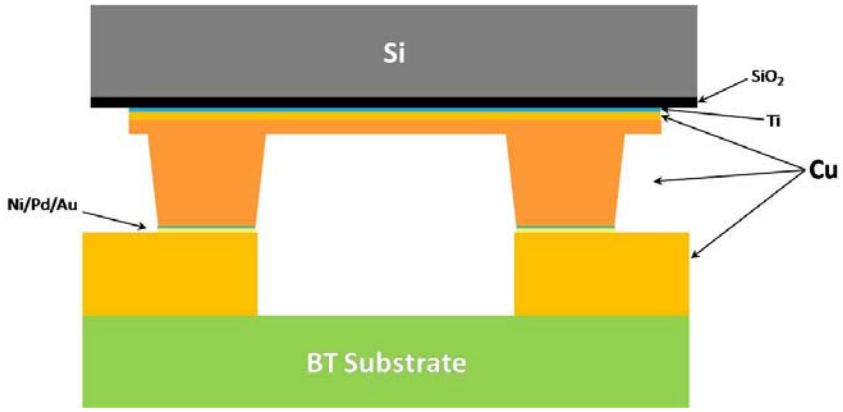


Figure 33. Close up schematic of Cu-Cu interconnection

Black's Model [11] shows that activation energy also affects the lifetime of interconnections under high current and temperature stress. An interconnection with high activation energy for electromigration has a longer MTTF. There have been numerous studies [49-57] exploring activation energy for electromigration in Cu and SAC solders, showing a range of 0.7-1eV for Cu and 0.64-1.1eV for Pb-free solders. In the aforementioned studies, pure Cu and electroplated Cu were investigated under electromigration. For the Pb-free solders investigated, both Cu and Ni UBM were used.

With all the above and published information available regarding Cu and solder-based interconnections, it can be concluded that Cu is an ideal choice as an interconnection material. The superior electrical and thermal properties of Cu enable it to handle high current densities and joule heating. In addition, the proposed Cu-Cu technique is a simple interconnection architecture, which reduces the likelihood of failure.

CHAPTER 3

EXPERIMENTAL TEST SETUP

This chapter describes the design, fabrication, and assembly of the test vehicle. The experimental setup and parameters for current density testing are also discussed.

3.1 Test Vehicle Design and Fabrication

3.1.1 Die Design and Fabrication

The die was designed to confirm the thermo-mechanical reliability and electromigration resistance of the Cu-Cu interconnection system. The pitch size and number of I/Os was in line with ITRS projections which anticipate 100µm pitch flip chip interconnections at an I/O density of 207-1100 pin-counts within the next two years. Consistent with this, on a 5mm x 5mm die, 760 bumps were arranged in an area-array format at a bump diameter of 30µm and minimum bump pitch of 100µm.

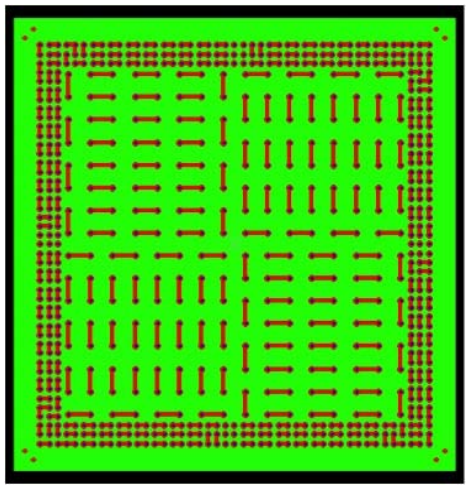


Figure 34. Test vehicle die design showing bump layout

The dies were fabricated using a standard semi-additive process on 550µm thick 6” silicon wafers. The wafers were first cleaned to ensure they were free of

contamination using standard CMOS cleaning processes. This included keeping the wafer in Piranha solution (10:1:100 solution of H_2SO_4: H_2O_2: H_2O) for 20 minutes at 120°C and then rinsing with de-ionized (DI) water.

3.1.1.1 Insulation and Seed Layer

The insulation layer was created by depositing silicon dioxide (SiO_2) using plasma-enhanced co-vapor deposition (PECVD). The purpose of this layer is to serve as insulation between the conductive silicon substrate and the subsequent conductive layers built on top of it. After deposition of the SiO_2 layer, titanium and Cu seed layers were deposited using a direct current (DC) sputterer. Initially, Ti was sputtered at a thickness of 30nm and then Cu at a thickness of 500nm. The Cu seed layer is created for subsequent electroplating of the structures with the Ti acting as an adhesion layer for the SiO_2 and Cu seed layer.

Table 15: Parameters for insulation layer

Parameter	Values
Machine	Plasma-Therm
Deposition Rate	50 nm/min
Time	40 min
SiH_4/N_2O flow rate (sccm)	100 / 900
Power	25 W
Temperature	250 °C
Total Thickness	2 μm

Table 16: Parameters for seed layer

Parameter	Values
Machine	CVC DC Sputterer
Titanium	
Deposition Rate	1 A/sec
DC Voltage	240 V
Current	1.4 A
Watts	340 W
Titanium Thickness	30 nm
Copper	
Deposition Rate	5-6 A/sec
DC Voltage	415 V
Current	2.4 A
Watts	1000 W
Cu Thickness	500 nm

3.1.1.2 Metal 1- Dog Bone Layer

Once the seed layer was constructed, photolithography was used to create the pattern for the first metal layer, which is referred to as the "dog bone" layer. The dog bone is equivalent to a redistribution layer which serves as a pad for the Cu bumps. SC 1827 positive liquid photoresist was first spin-coated on the wafers followed by a pre-bake at 105°C for 3 minutes. Using a dark-field mask, the wafers were exposed to UV light in a Karl-Suss MA6 mask aligner (h-line 405 nm) for 27 seconds to create the desired patterns. The wafers were developed in MF319 solution for 1.5 minutes. The final mold thickness was ~4-5µm to achieve a dog bone height of ~2-3µm.

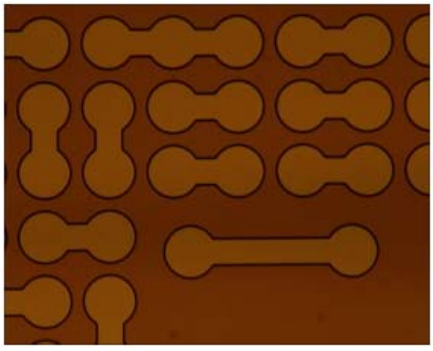


Figure 35. Photoresist mold of the dog bone structure

Table 17: Photolithography parameters of dog bone layer

Parameter	Values
Photoresist Application	
Machine	Karl Suss RC8 Spin Coater
Resist	SC 1827 Positive Photoresist
Spin Speed	500 RPM/1000 RPM Ramp rate: 5 sec 1000 RPM/100 RPM Ramp rate: 40 sec
Prebake	105°C for 3 min
Exposure	
Machine	Karl-Suss MA6 Mask Aligner (h-line 405 nm)
Exposure Dose	620 mJ/cm^2
Intensity	23 mW/cm^2
Exposure Time	27 sec
Developer	
Solution	MF319
Time	1.5 min

After photolithography was completed, an in-house Cu electroplating bath was used with Techno Copper P75 chemistry. The components needed to make the solution are included in the table below.

Table 18: Components of the Cu electroplating bath

Parameter	Optimum Value
Copper Sulfate Pentahydrate	10 oz/gal
Sulfuric Acid	10% by volume
Chloride Ion	50 ppm
Techni PC-75 Brightener	0.5% by volume
Techni PC-75 Carrier	0.5% by volume
Temperature	75°F
Current Density	30 amps per square feet (ASF)
Anode to Cathode Ratio	2 to 1

The steps used to create the Cu electroplating bath are listed below:

1) Fill the plating tank with DI water equal to 20% of final total volume: 20 gallons/100 gallons
2) Add liquid Copper Sulfate Pentahydrate: 27.8 gallons/100 gallons of solution
3) Add Sulfuric Acid: 10 gallons/100 gallons of solution
4) Analyze for chloride ion and adjust to 50ppm
5) Cool solution to 100°F or less before adding Techni Copper PC-75 Carrier and Brightener: 0.5 gallon/100 gallons of solution of each component
6) Bring to final volume with DI water

Before starting through-resist plating of the dog bone layer, a dummy board was put in the Cu bath to ensure good plating quality. The dummy board, coated with electroless Cu, was initially put inside of an acid dip for 1 minute and then transferred to the electrolytic bath. A square rack was used to hold the dummy board as well as the 6" wafers to ensure that it was secure during the electroplating process.

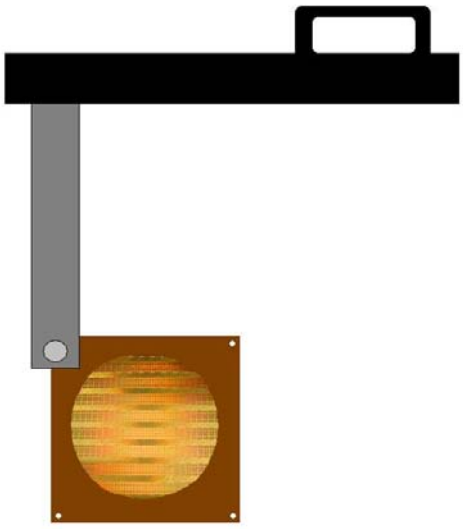


Figure 36. Rack system used to hold wafer through electroplated process

For the dummy board, a current of 4A for 1 hour was applied. The air agitation (N2), vibration, and heat (22°C) were turned on during the process for good uniform

plating. After electroplating was completed, the dummy board was rinsed with DI water and inspected for contamination. The 6" wafers were then put through the same process steps. However, the plating time was for 15-17 minutes with an applied current of 4A, equivalent to ~2.85 amps per square decimeter (ASD). The final thickness of the Cu dog bone pad was around 2-3μm which was determined by using a Dektak Profilometer and an Olympus LEXT 3D Material Confocal Microscope.

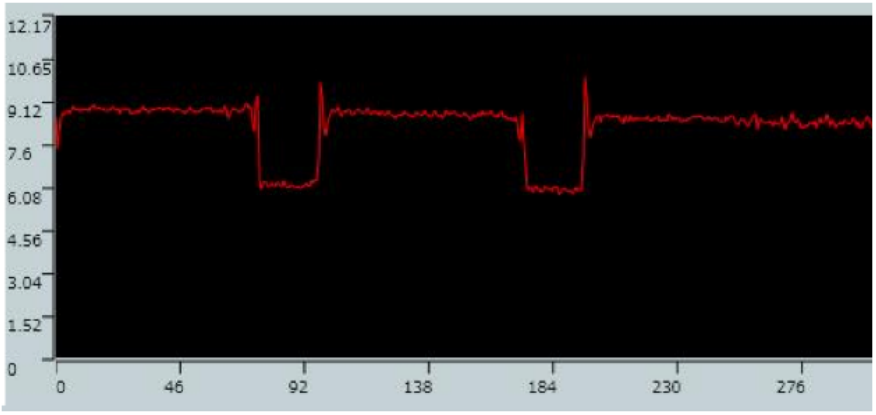


Figure 37. 3D laser-confocal profilometry showing ~ 3μm thickness for the dog bone metal layer

After the dog bone layer was plated, the liquid photoresist was removed by placing the wafers in acetone for 1 minute. The wafers were cleaned in a plasma-therm reactive ion etching (RIE) machine (Plasma Etch BT-1) with O_2 for 5 minutes to remove organic residue. They were then cleaned in 10% H_2SO_4 and nitrogen baked at 90°C.

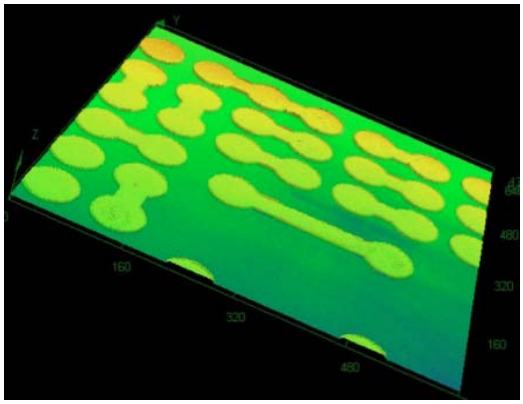


Figure 38. 3D image of wafers patterned with dog bone layer

3.1.1.3 Metal 2- Cu Pillar Bumps

To fabricate the second metal layer, or Cu pillar bumps, the dog bone plated wafers were first laminated with a dry film photoresist. A dry film photoresist was used due to its low cost, no pre or post baking, and high throughput process capability with low material waste. Dupont's MXA115 negative dry film photoresist is 15µm thick, which was conveniently chosen to achieve a desired bump height of ~12-15µm. The MXA115 photoresist is also beneficial due to its low aspect-ratio which makes it tolerant to over-exposure. The developing time was crucial given that over-developing causes delamination. Using a DF-4200 14" hot-roll laminator, the photoresist was laminated at 120°C. The wafers were exposed in a Karl-Suss MA6 mask aligner (i-line 365 nm) for 8-13 seconds and developed in 3% Na_2CO_3 aqueous solution for 2 minutes.

Before electroplating the Cu pillars, the wafers were again subjected to plasma-therm RIE to get rid of photoresist residual, which can hinder the Cu plating process. The same in-house Cu electroplating bath and process used for the dog bone layer was employed to fabricate the Cu pillar bumps. The wafers were put inside of an acid bath for 1 minute and then transferred to the electroplating Cu bath. An applied current of 6A, equivalent to 4.75 ASD, and a plating time of ~17-20 minutes was used to attain a Cu pillar height of ~12-15µm. To remove the MXA115 photoresist, the wafers were submerged in diluted Enthone PC 4025 resist stripper at 50-70°C and were agitated by hand for 1-2 minutes. The Cu seed layer was removed using Cu etchant (1:3:30 solution of H_2SO_4: H_2O_2: H_2O) for 30 seconds and the Ti layer was removed with 5% hydrofluoric acid (HF) solution for 4-5 seconds. The complete process flow showing each step for wafer fabrication is shown in Figure 39.

Table 19: Photolithography parameters of Cu pillar bumps

Parameter	Values
Photoresist Application	
Machine	Think and Tinker, Ltd. DF-4200 14" hot-roll laminator
Resist	MXA115 Negative Photoresist
Temperature/Conveyer Speed	120°C / 2
Exposure	
Machine	Karl-Suss MA6 Mask Aligner (i-line 365 nm)
Exposure Dose	190 mJ/cm^2
Intensity	8.5 mW/cm^2
Exposure Time	8-13 sec
Developer	
Solution	3% Na_2CO_3 aqueous solution
Temperature	85°C
Time/Conveyer Speed	2 min / 40

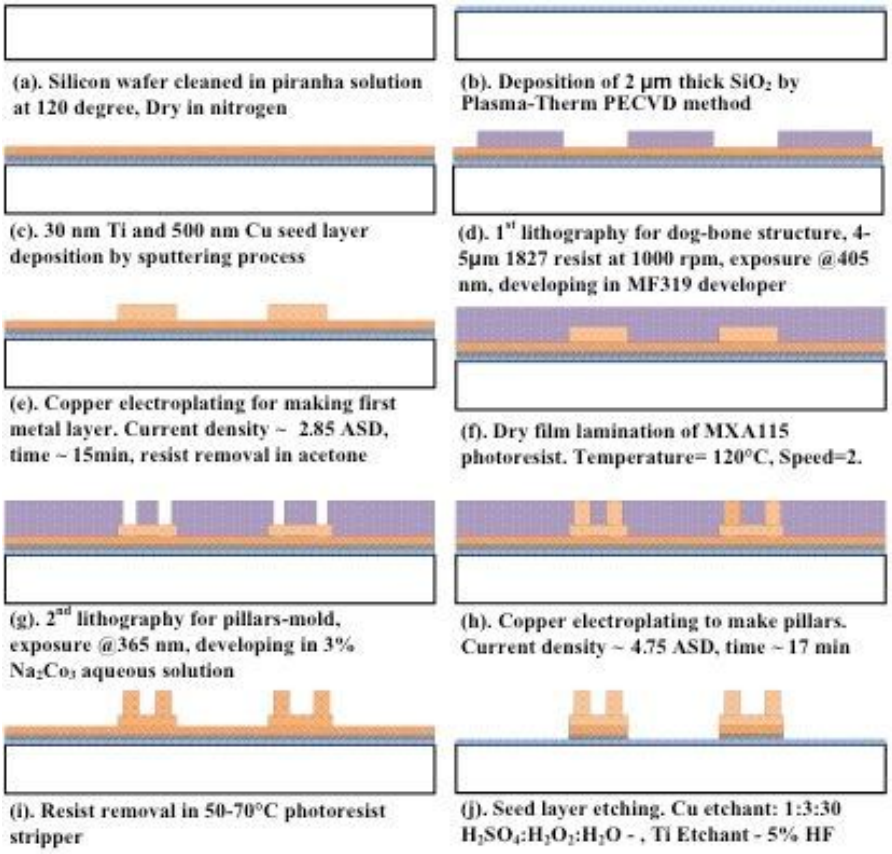


Figure 39. Process flow for 6" wafer fabrication

3.1.1.4 ENEPIG Surface Finish

Electroless nickel, electroless palladium, and immersion gold (ENEPIG) surface finish was coated on the wafers to prevent oxidation of Cu. The ENEPIG surface finish process came into the industry in the late 1990s. In recent years, it has become more popular than previous surface finishes because of its compatibility with lead-free processes and ability to meet new packaging reliability needs. ENEPIG has more than 12 months of shelf life, excellent solder joint reliability, and the capability to be used as a contact surface. The main reason ENEPIG is better than electroless nickel immersion gold (ENIG) surface finish is because it overcomes the "black pad" issue which arises due to excessive corrosion of the nickel surface during immersion gold. This causes a high concentration of phosphorus in the nickel, which is attributed to the failure of the solder joints. Moreover, ENEPIG is more beneficial since the palladium works as a barrier layer to reduce Cu diffusion to the surface [58].

ENEPIG surface finish was completed using Aurotech chemistry and process developed by Atotech [59]. The achieved plating thickness values were 1-2μm nickel (Ni), 0.1-0.2μm palladium (Pd) and 0.03-0.06μm gold (Au). The time and temperature used for each step is shown in Table 20. Before committing the actual wafers to the ENEPIG process, dummy plating was once again completed.

Table 20: ENEPIG process steps

Solution	Time	Temperature
Oxide Clean	2.5 min	40°C - 50°C
Rinse with DI water		
MicroEtch	30 sec	25°C
Rinse with DI water		
Acid Dip	1 min	25°C
No Rinse		
Activation	2 min	25°C
Rinse with DI water in separate tank		
Electroless Ni	5 min	80°C - 90°C
Rinse with DI water		
Electroless Pd	8 min	50°C - 70°C
Rinse with DI water		
Immersion Au	5 min	80°C - 90°C
Rinse with DI water		

Table 21: Contents of each component used for ENEPIG surface finish

	Make-Up of 500mL	Volume (mL)
1) Oxide Clean	DI water	377.5
	H_2SO_4	22.5
	Pro Select SF conc.	100
2) MicroEtch	DI water	232.5
	MicroEtch SF conc.	37.5
3) Acid Dip	DI water	237.5
	MicroEtch SF conc.	12.5
4) Activator	DI water	237.5
	MicroEtch SF conc.	12.5
5) Ni (Adjust pH to 4.8 with NH_4O_4)	DI water	2000
	CNN Makeup	375
	Part A (CNN Replenisher)	150
	NH_4O_4	40
6) Pd (Adjust pH to 5.5 with 10 % H_2SO_4 or 10 % KOH)	DI water	1875
	PD-Tech PC Reduction	375
	PD-Tech PC Plus Makeup	250
7) Au (Adjust pH to 5.5 with 10 % H_2SO_4 or 20 % KOH)	DI water	1900
	Aurotech SF Plus Makeup	595
	Potassium Gold Cyanide	7.325 grams
	Aurotech SF Starter	2.5

The first step was an oxide-clean, which is an acidic-wetting solution used for the preparation and cleaning of the Cu pillars. The second step included micro-etching to clean the Cu surface by slightly roughening it. The resulting Cu had a uniform and fine-grain etch, which resulted in an optimal bonding surface for Cu and the subsequent layer. The micro-etching solution also had a slow etching rate to ensure there was no excessive removal of Cu. The acid dip step was used to protect the Aurotech Activator 1000, used in the next step, from non-compatible drag-in. The fourth step was completed to activate the Cu pillar surface for Ni plating. It was composed of an acidic Pd activation system based on sulfuric acid. The last three steps included plating Ni, Pd, and Au. Aurotech's nickel bath was used to deposit uniform nickel-phosphorous alloy which consisted of 7-10%, by weight, of phosphorus. Pd was plated to protect the Ni from getting attacked by Au. To finish the ENEPIG surface finish process, a thin layer of Au was deposited on the Ni/Pd [59].

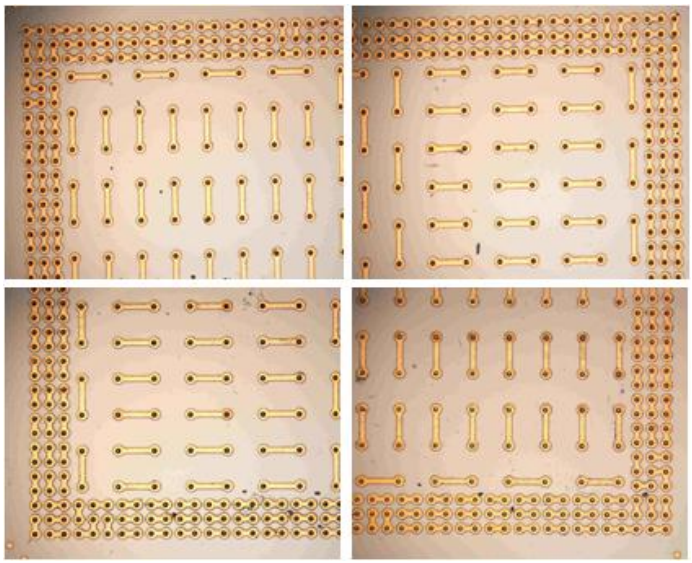
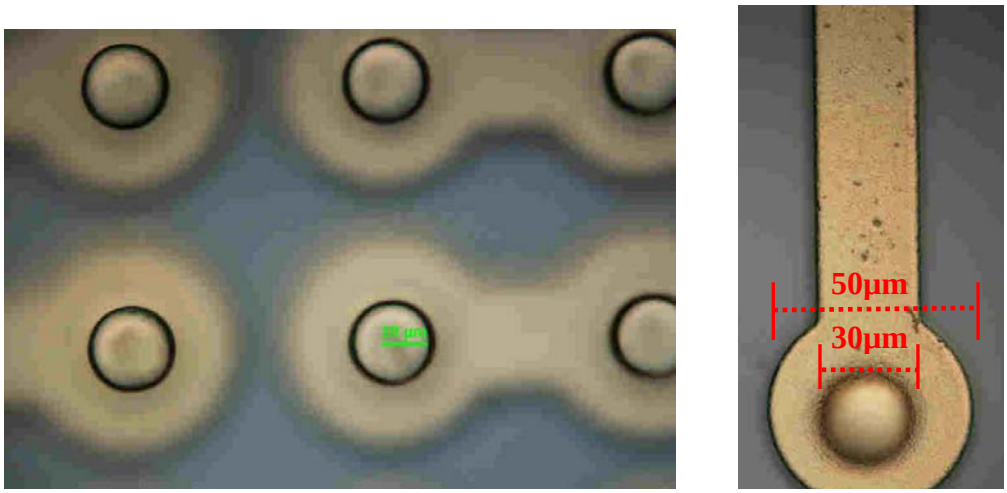


Figure 40. Optical microscope image of a single die with ENEPIG surface finish

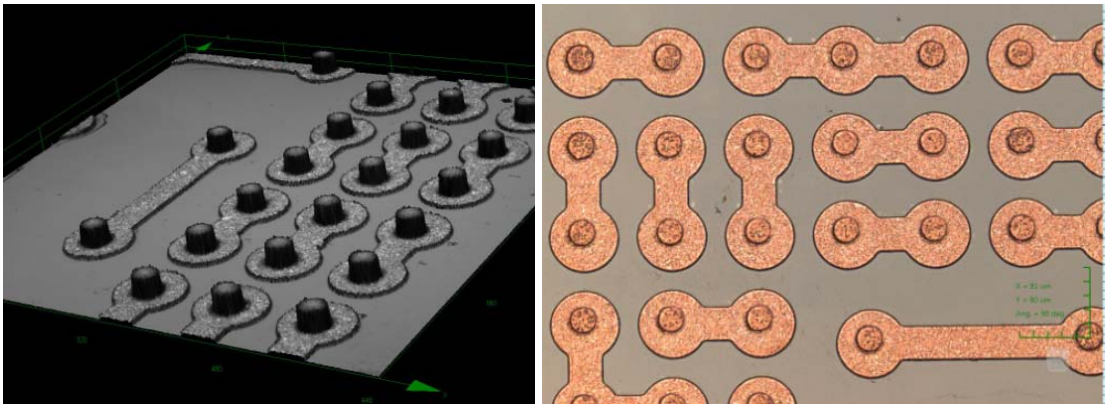


(a) **(b)**

Figure 41. Optical microscope image at 50X focused on the (a) 30µm bumps and (b) the dog bone

3.1.1.5 Analysis of the Dog Bone and Bump Structures

After the wafers were fabricated, 3D microscopy was used to analyze the dies. Several measurements were taken of around 3-5 bumps to ensure the desired heights were obtained for both metal layers. The average dog bone height of the wafers was ~2.3-2.7µm and the average Cu pillar bump height was ~12-15µm.



(a) **(b)**

Figure 42. A 3D microscope image of the dog bone layer with Cu pillar from a (a) side view and (b) top view

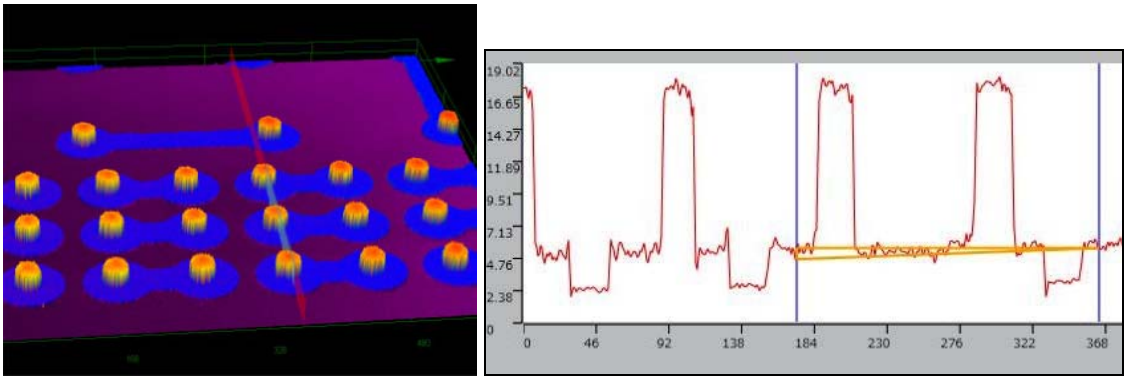
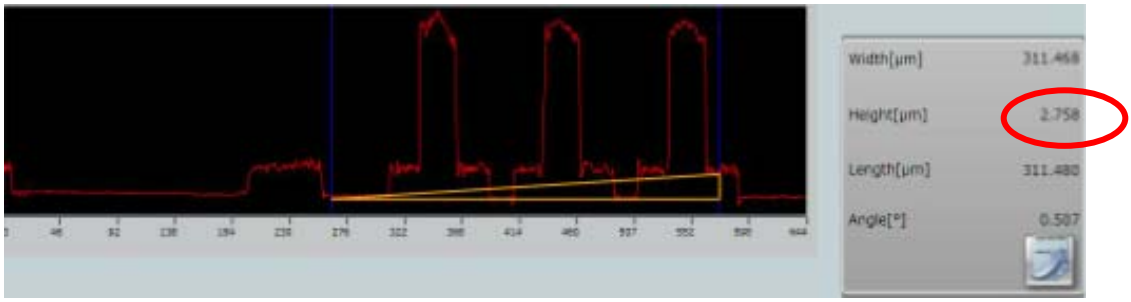
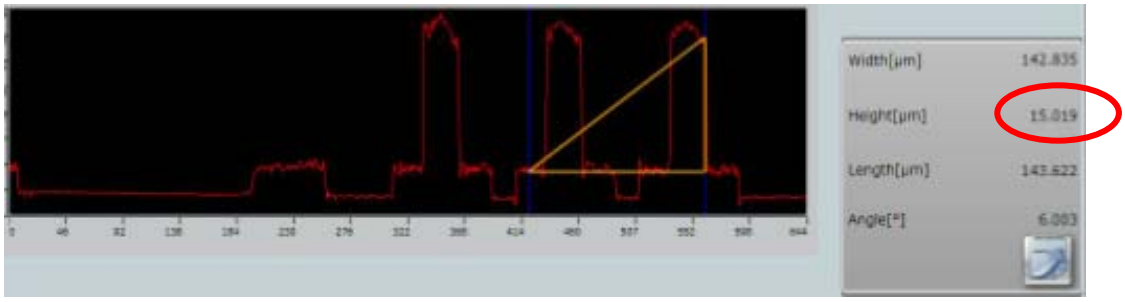


Figure 43. A 3D microscope image showing an average roughness of ~1µm for the Cu pillars



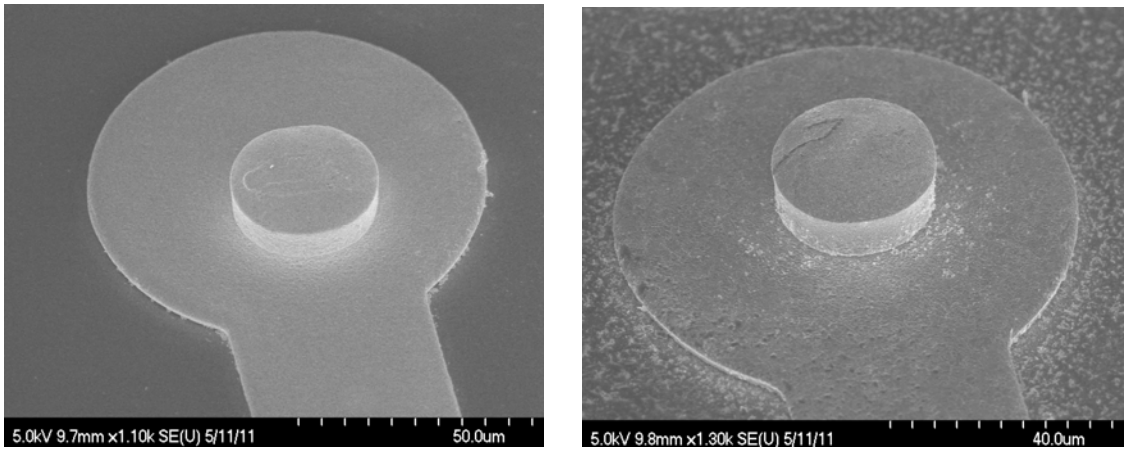
(a)



(b)

Figure 44. Images of 3D laser-confocal profilometry showing (a) dog bone and (b) Cu pillar height

After examining the height of the dog bone and Cu pillar bumps, a Scanning Electron Microscope (SEM) was used to study the shape of the pillars. The images below show a dog bone and Cu pillar with and without ENEPIG surface finish. The images prove that the shape of the pillar is nearly cylindrical, as desired.



(a) **(b)**

Figure 45. SEM images of a dog bone and Cu pillar bump (a) with ENEPIG and (b) without ENEPIG

3.1.2. Substrate Design and Fabrication

The substrate was designed to assist in probing the daisy chains of the package using 24 pads to evaluate the bump resistances during TCT and current density testing. The package consisted of 4 corner daisy chains, 8 edge daisy chains, and 4 center daisy chains. The substrate size was 15mm x 15 mm and was fabricated without a cavity with both RXP and BT materials.

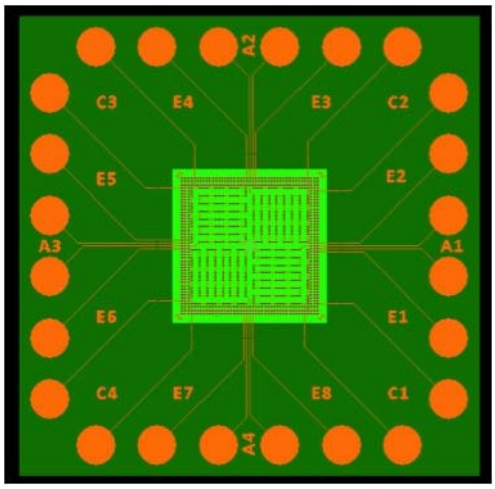


Figure 46. Substrate design showing 24 probe pads and 16 daisy chains

RXP was a new substrate material originally chosen by GT-PRC to allow for the embedding of dies with 30µm ultra-fine pitch. The substrate consists of a 100µm, low loss, and thin core laminate (RXP-1) with a 20µm low dielectric constant build-up film (RXP-4). The RXP-1 is a glass-reinforced hydrocarbon polymer and high transition temperature (Tg) laminate core. It has excellent thermal stability as it has a high Tg of more than 300°C, making it ideal for high temperature interconnections such as lead-free solders. It has low moisture absorption and a CTE of around 10-15ppm/°C, which helps reduce the stress on first level interconnections from the chip. The RXP-4 material is the build-up dielectric which allows for low RF signal delay and very low RF power loss during signal transmission through the material. Its dielectric constant is less than 3 and it also has fairly low moisture absorption [60]. The addition of BT, as a substrate material, was because of its popularity in the packaging industry. The BT material also has a high Tg greater than 300°C and a very low dielectric constant. It has a low CTE of 15ppm/°C as well as excellent electrical insulation in high humidity and temperatures [61].

Both the RXP and BT material had Cu cladding on top of them with an initial thickness of ~12µm. The substrates were cut into several 6in x 6in panels and fabricated through a subtractive etching process to create the desired patterns. They were also coated with ENEPIG surface finish. For the RXP substrates, the build-up layer had to be laminated first to the RXP-1 core by using a hot press. This was completed by initially baking the RXP-1 and RXP-4 materials at 100°C to remove moisture. The RXP-4 was then placed on both sides of the RXP-1 and put inside of a stack-up of aluminum, rubber, and steel plates to protect it inside of the hot press, depicted in Figure 47. The load on the hot press was adjusted to 6.5 tons and the temperature was set to 450°F. Once it reached 450°F, the stack-up was kept inside of the hot press for 2 hours. The hot press was then turned off and cooled down to 65°F. The pressure was decreased and the stack up was taken out of the hot press carefully.

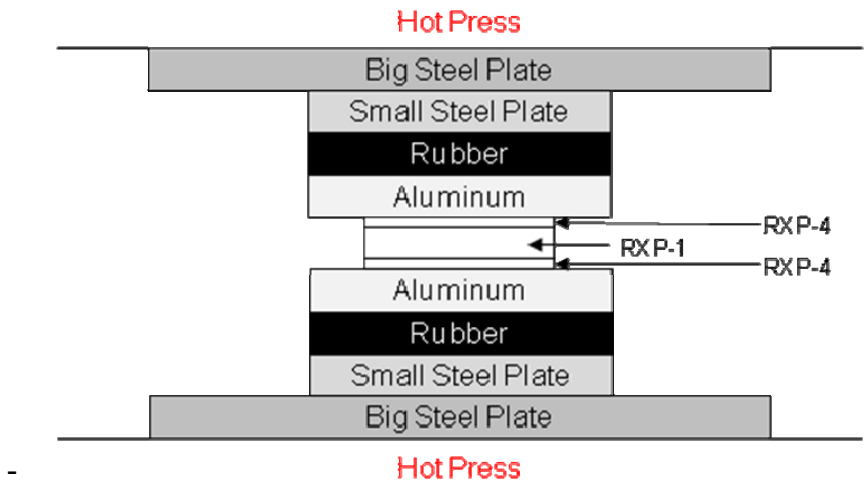


Figure 47. Stack-up layer inside of hot press to laminate RXP-4 build-up layers on RXP-1 core

The subtractive etching process was similar for both RXP and BT. The substrates were subjected to micro-etching for 10 seconds, using an in-house lab setup, followed by a nitrogen bake at 120°C for 20 minutes. The hot-roll laminator was used to laminate MXA115 photoresist on both sides of the substrate at a temperature of 120°C. Both sides of the substrate were exposed at an intensity of 20mW/cm^2 for 5 seconds to achieve an exposure dose of 100mJ/cm^2. They were subsequently developed in 3% Na_2CO_3 aqueous solution at 85°C.

Once the desired pattern was created through photolithography, the unwanted Cu was removed using a Cu etchant solution (2.5: 5: 17.5 solution of HCl: H_2O_2: $CuCl_2$) at a temperature of 115°C. The only fabrication step that differed between the RXP and BT substrates was the etching speed. For RXP, the front side was exposed three times to the Cu etchant at conveyer settings, in inches per minute, of 20, 60, and then 60 once more. Each of these exposures was performed at a different orientation, allowing for uniform etching. The back side was also exposed three times at conveyer settings of 20, 60, and 60 with the orientations once again changed each time. The BT etching speed was simpler. The front and back side was exposed at a conveyer speed of 20.

The diluted Enthone photoresist stripper was once again used to remove the MXA115 at 50-70°C for 1-2 minutes. The process flow illustrating the subtractive etching process is shown in Figure 48. Using the same ENEPIG process flow, mentioned in the previous section, the substrates were plated with Ni, Pd, and Au for 20, 8, and 10 minutes, respectively. Figures 49-52 show optical microscope images of fabricated coupons using both BT and RXP.

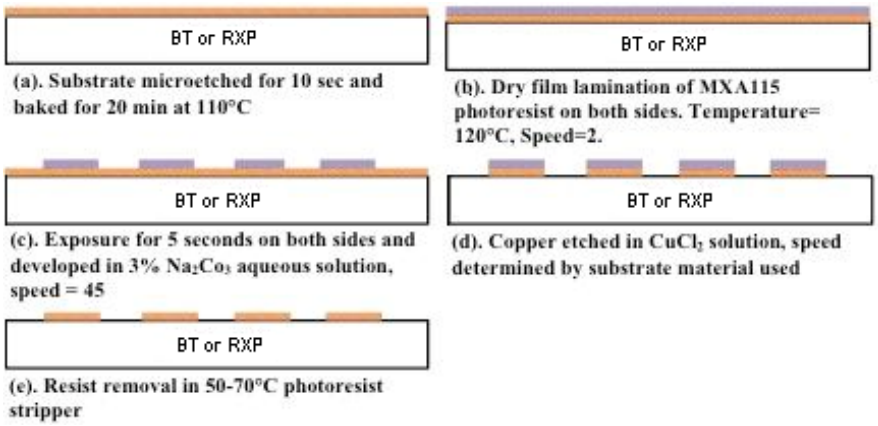


Figure 48. Process flow showing fabrication process for 6in x 6in substrate panels of RXP and BT

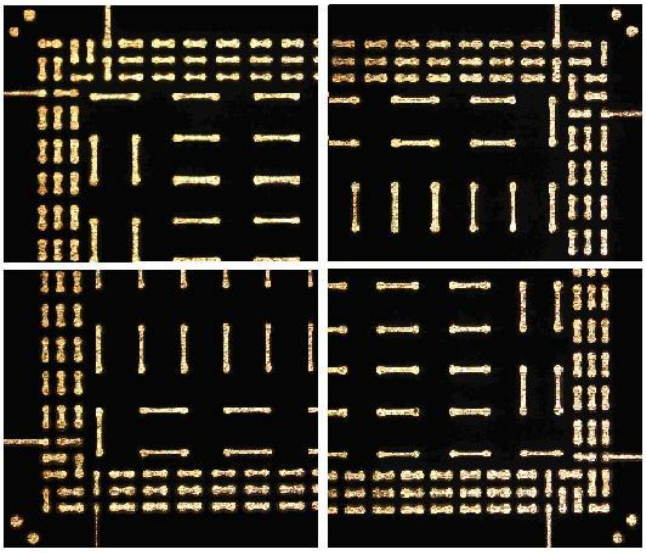
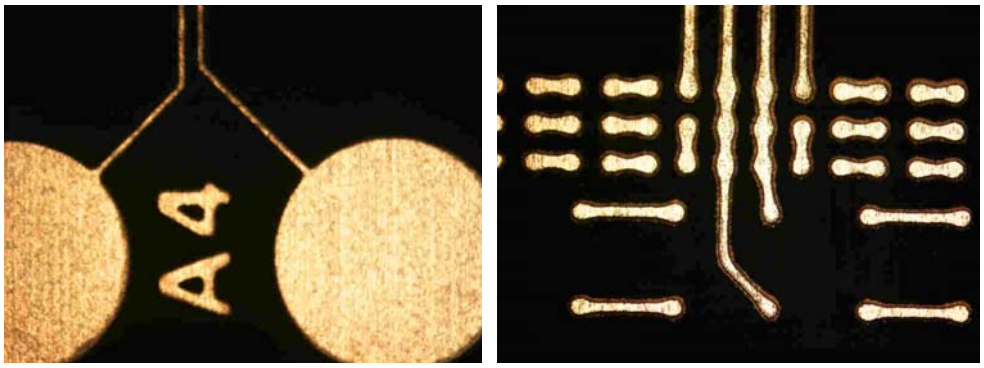


Figure 49. Optical microscope image of the four corners of the test vehicle substrate coupon using BT



(a) **(b)**

Figure 50. Optical microscope image of (a) probe pads and (b) traces leading to a center daisy chain of the test vehicle substrate coupon using BT

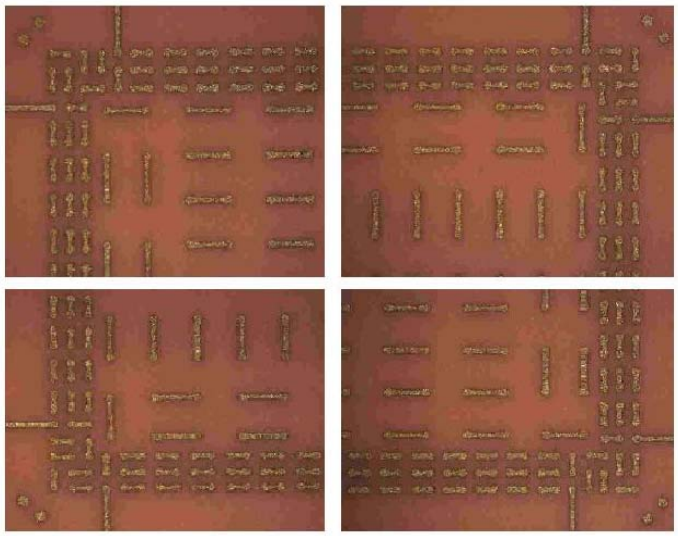
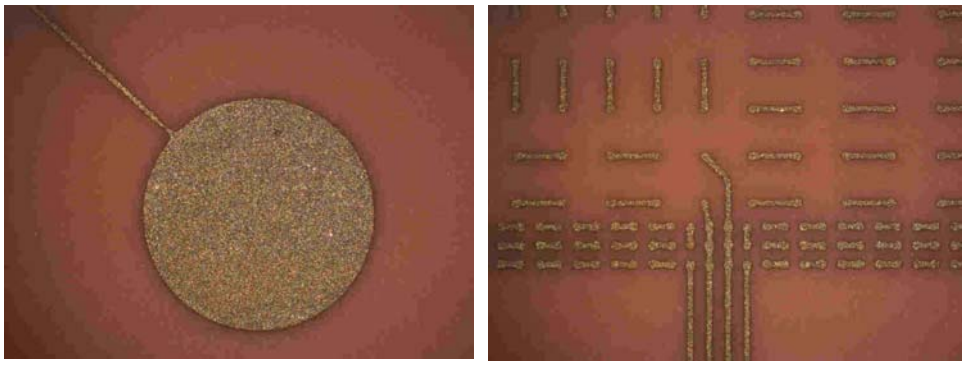


Figure 51. Optical microscope image of the four corners of the test vehicle substrate coupon using RXP



(a) **(b)**

Figure 52. Optical microscope image of (a) probe pad and (b) traces leading to a center daisy chain of the test vehicle substrate coupon using RXP

3.2 Assembly Process for Area-Array Test Vehicle

The test vehicles were assembled using a FINETECH Fineplacer© Lambda assembly tool with an alignment accuracy of +/-1µm. The first step included applying NCF to the substrate and pre-bonding it at 90°C. The NCF is an epoxy-based material that was applied to bond the die to the substrate. Once the NCF was placed, the carrier tape on top of the NCF was removed at room temperature. The die was aligned with the substrate by alignment markers, which were present on opposite corners of both the die and substrate. Once aligned, the die was placed on the substrate at 90°C.

The last step was thermocompression bonding at 180°C with an applied load. The amount of load implemented was critical in providing high reliability. Previously for the peripheral interconnection test vehicle, an effective bump pressure of 300MPa was employed to provide proper bump-to-pad deformation in order to pass more than 1000 cycles of TCT, as shown in Table 7 in Chapter 1 [36]. For the area-array test vehicle, the load needed to equal 300MPa of pressure was calculated to be 161N. This was determined by taking into account the number of bumps as well as the cross-sectional area of the bumps. However, the Finetech tool had a maximum load capability of only 100N and in order to keep a margin of safety, only 80N was applied to the samples.

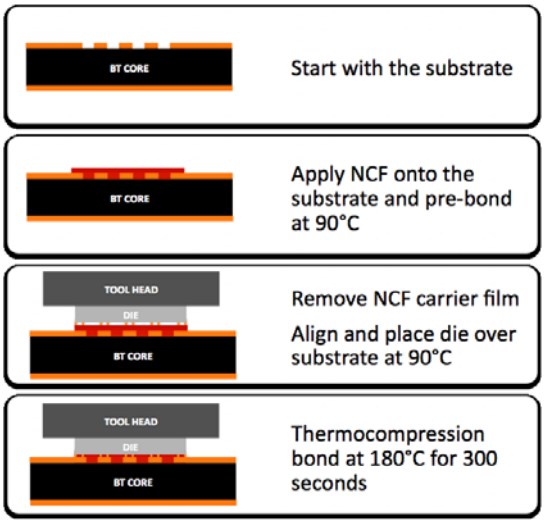


Figure 53. Process flow for assembly of area-array test vehicle

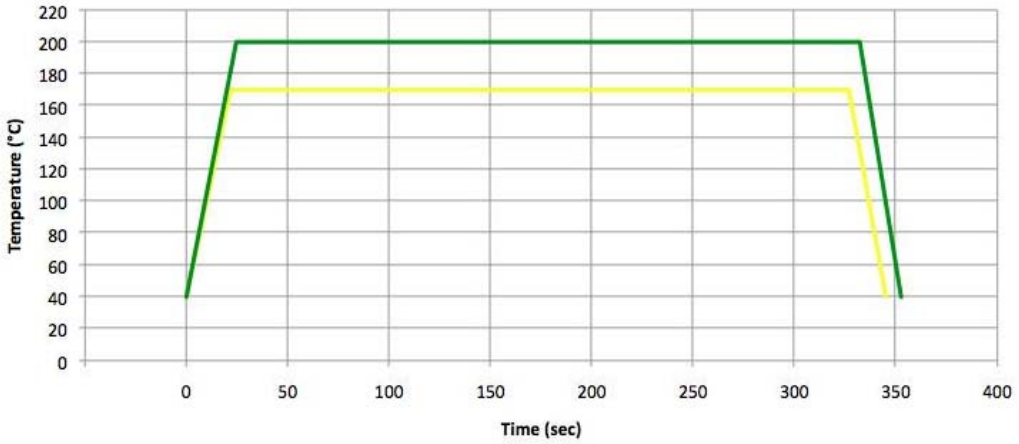


Figure 54. Temperature profile used during thermo-compression bonding

3.3 Electromigration Testing of Cu-Cu Interconnections

To investigate the electromigration reliability of the 30µm diameter Cu-Cu interconnections, assemblies were subjected to accelerated test conditions of high current and temperature. The testing parameters included an applied current density of 10^4-10^6 A/cm^2 at a temperature of 130°C. Both manual and automatic test setups were utilized depending on the current source.

The first test at 10^4 A/cm^2 was conducted through a manual setup using a Keithley 236 Source-Measure Unit. Constant current was supplied to the corner daisy chain of a BT area-array test vehicle, which consisted of 14 bumps in series. Based on the bump-to-pad contact area, the calculated amount of current needed to achieve 10^4 A/cm^2 was 70.68mA. The sample was kept in an Espec thermal chamber at a constant temperature of 130°C and voltage measurements were taken manually every 24 hours to calculate the resistance of the corner daisy chain. A 50% increase in resistance was declared a failure for all three electromigration tests.

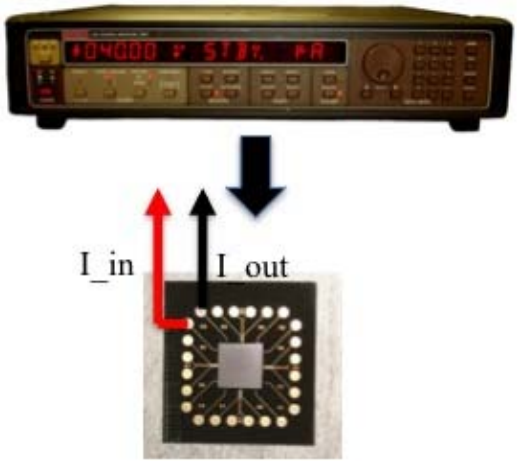


Figure 55. Manual test setup for current density testing at 10^4 A/cm^2

The second test at 10^5 A/cm^2 was completed through an automatic setup using a Keithley 2400 Source Meter, which communicated with a computer via MATLAB to obtain resistance measurements every 30 minutes. The calculated current was 0.7068A, which was supplied to a corner daisy chain of another BT sample placed inside the thermal chamber at 130°C.

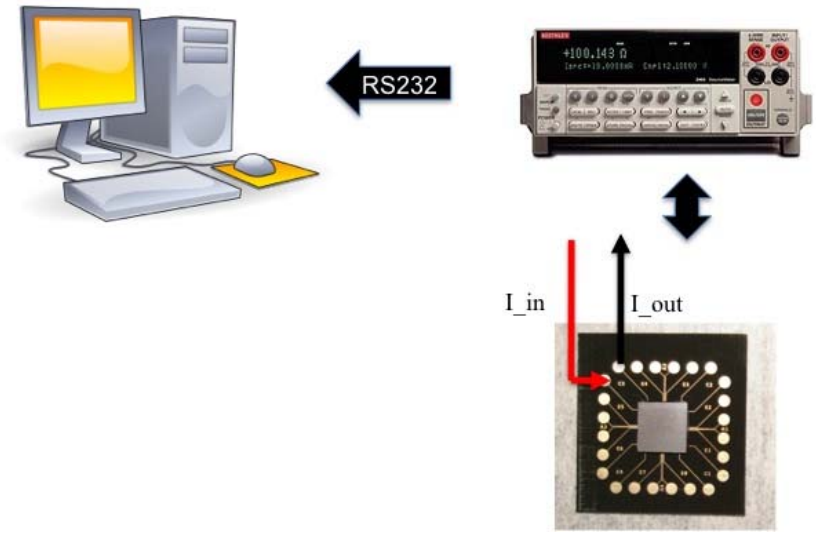


Figure 56. Automatic test setup for current density testing at 10^5 A/cm^2

The third test at 10^6 A/cm^2 was also performed with a manual setup. A peripheral interconnection test vehicle was used this time to reduce the amount of current needed to

achieve 10^6 A/cm^2 of current density. The peripheral interconnection test vehicle consisted of 15µm diameter bumps whose cross-sectional area was four times smaller than the bumps in the area-array test vehicle. An Agilent U8002A DC Power Supply was used to deliver 1.76A of current to a corner daisy chain, which consisted of one single bump. In order to get better voltage measurement resolution than what the Agilent U8002A could provide, another HP 3478A Multimeter was put in parallel. Once again, the voltage measurements were taken every 24 hours to calculate the corner daisy chain resistance of the sample.

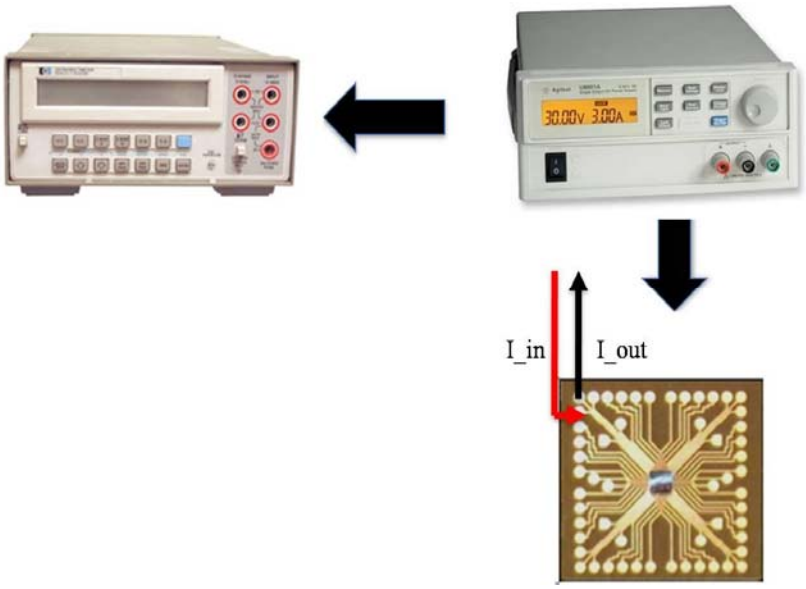


Figure 57. Manual test setup for current density testing at 10^6 A/cm^2

CHAPTER 4

RESULTS AND DISCUSSION

This chapter discusses the thermo-mechanical reliability and electromigration results obtained for the Cu-Cu interconnections. The packages were subjected to TCT and periodically examined with C-SAM and cross-sectioning. In addition, electromigration testing was completed to analyze the interconnections under high current and temperature stress.

4.1 Thermo-mechanical Reliability

The proposed Cu-Cu interconnection technology has already been proven highly reliable with peripheral bumps at 30µm pitch [36]. Therefore, the objective was to validate the thermo-mechanical reliability of high I/O area-array packages. The area-array test vehicle, discussed in Chapter 3, was assembled with BT substrates and the following steps were taken to investigate the Cu-Cu interconnections before and after thermal cycling.

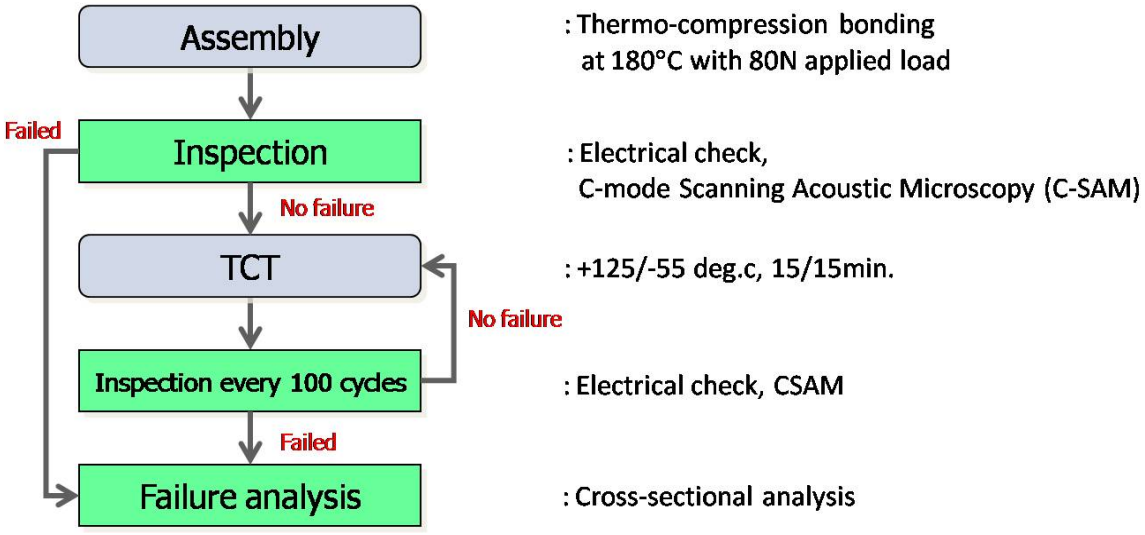


Figure 58. Process flow used to examine the Cu-Cu interconnections for thermo-mechanical reliability

4.1.1 Initial Assembly Results and C-SAM Inspection

Following the process in Figure 58, the first step was determining the initial assembly results through electrical examination of the packages. This was completed by probing the pads on the substrate to evaluate the 16 daisy chain resistances, as seen in Figure 59.

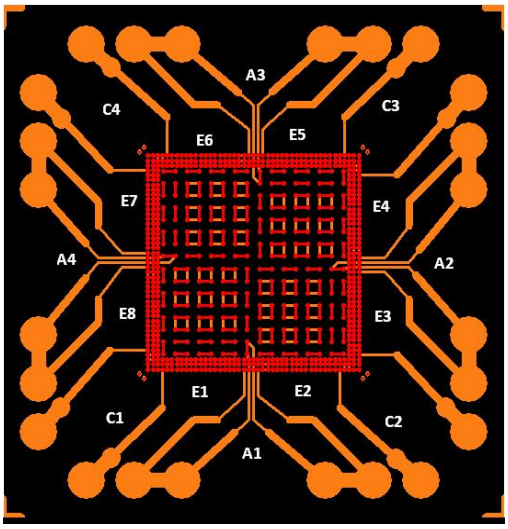


Figure 59. Test vehicle daisy chain layout with die and substrate aligned

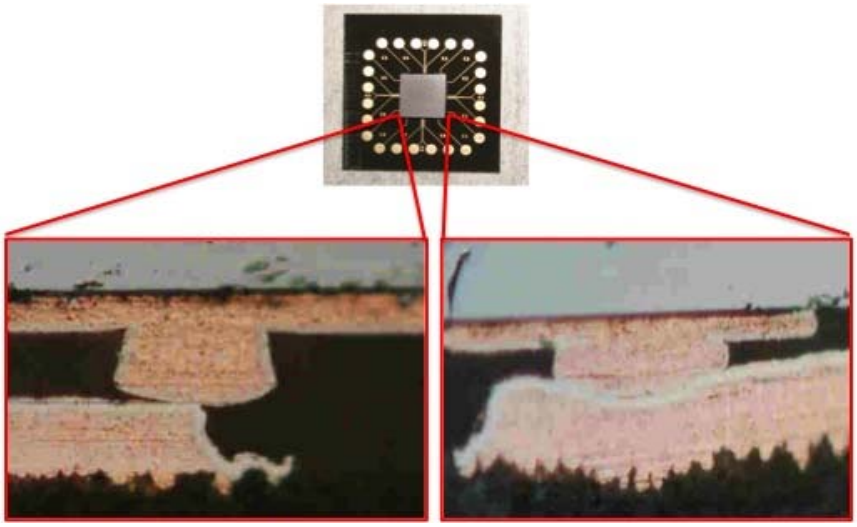
After assembly, some daisy chains showed poor resistance. In addition, only half of the daisy chains were connected while the other half were not. C-SAM was then used to identify defects before TCT, which showed voiding across the assembly. To properly investigate these abnormalities, the root cause of failure was determined.

4.1.1.1 Root Cause Analysis after Assembly

The reason for poor daisy chain resistance was attributed to insufficient deformation of bump-to-pad. As previously mentioned, 300MPa of effective bump pressure is needed to attain proper bump-to-pad deformation, which is required to achieve high reliability for more than 1000 cycles of TCT [36]. However, the load limitation of the Finetech tool resulted in only 80N of applied load during thermo-

compression bonding, equivalent to about 150MPa. This was not enough to achieve proper deformation, which is required to obtain good daisy chain resistance.

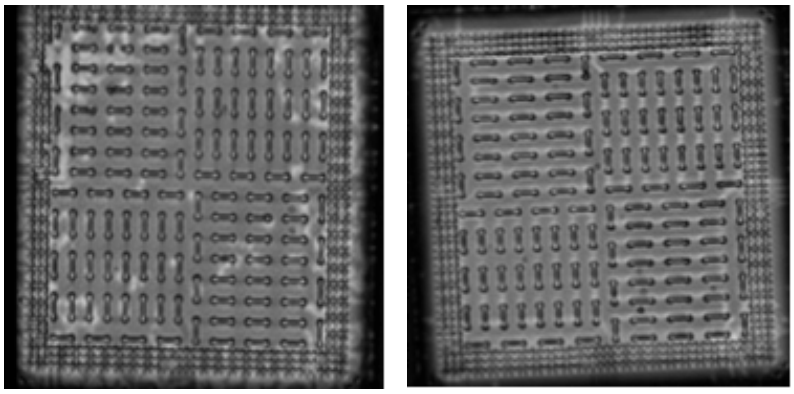
To investigate the reason for partially-connected dies, cross-sectional analysis was completed on one of the assemblies. The cross-section, in Figure 60, showed that the corner daisy chain with good resistance had proper deformation of bump-to-pad. However, the side with no electrical connection did not show any deformation. This discrepancy proved that there was a tilt in the tool head of the Finetech tool used during assembly. In order to compensate for the tilt, a gimble tool head was used to provide pre-leveling and automatic leveling. The number of working daisy chains increased, but a fully connected assembly was still not attained.



(a) **(b)**

Figure 60. Cross-section of partially-yielding die showing (a) no deformation on the left edge and (b) proper bump-to-pad deformation on the right edge

Insufficient load also resulted in voiding during C-SAM. To overcome this issue, an additional NCF dry-up process was added at the beginning of thermo-compression bonding at 75°C for 2 minutes in order to remove any remaining solvents in the NCF. In addition, the die and substrate were cleaned with isopropyl alcohol (IPA) to remove any residue before assembly. The dry-up process and IPA cleaning drastically reduced voiding after assembly, as seen in Figure 61.

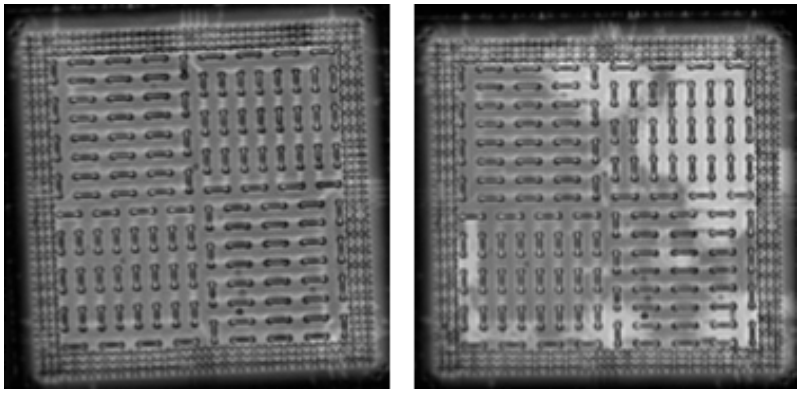


(a) **(b)**

Figure 61. C-SAM image of BT assembly (a) without NCF dry-up process and (b) with NCF dry-up process and IPA cleaning

4.1.2 Temperature Cycle Testing

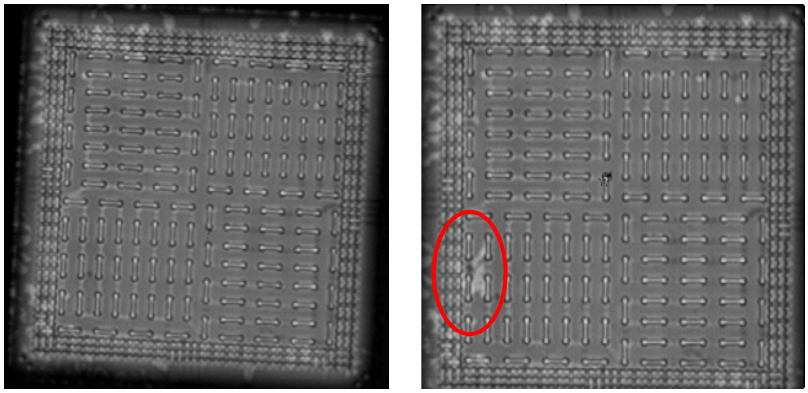
Although the assemblies were partially-connected, they were subjected to temperature cycling from -55°C to 125°C with a dwell-time of 15 minutes at each extreme temperature. The TCT process followed JEDEC standard JESD22-A104C (condition B) in order to evaluate the thermo-mechanical reliability of the Cu-Cu interconnections in the area-array test vehicle. After 500 cycles were completed, electrical examination showed failures in some of the daisy chains, as determined by a 50% increase in resistance. After repeating C-SAM, extensive voiding was observed, as seen in Figure 62.



(a) **(b)**

Figure 62. C-SAM image of BT assembly (a) after thermo-compression bonding and (b) after 500 cycles of TCT

After examining the assemblies with BT substrates, assemblies with RXP were subsequently examined under TCT. Similar to the BT samples, RXP showed voiding, but with less severity. This is seen in Figure 63. The samples with voiding were used for root cause analysis of the failure.



(a) **(b)**

Figure 63. C-SAM image of RXP assembly (a) after thermo-compression bonding and after (b) 500 cycles of TCT

4.1.2.1 Root Cause Analysis after TCT

In order to understand the reason for extensive voiding after TCT, cross-sectional analysis was performed. The cross-section in Figure 64 revealed that there was clear delamination at the die and NCF interface. The delamination was potentially the result of insufficient load and lack of an organic passivation layer on the die surface, which typically helps improve adhesion.

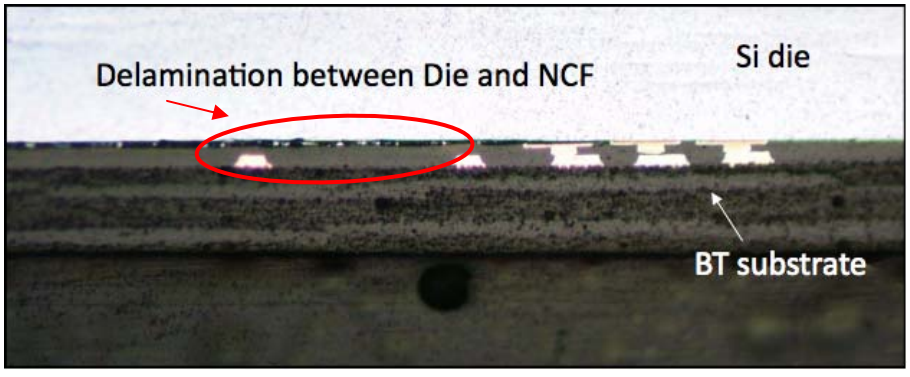


Figure 64. Cross-section of a BT assembly showing delamination between silicon die and NCF after TCT

4.1.3 Thermo-mechanical Reliability Results

Although there was insufficient load and delamination observed after TCT, assemblies with good initial daisy chain resistance survived more than 2000 cycles of TCT.

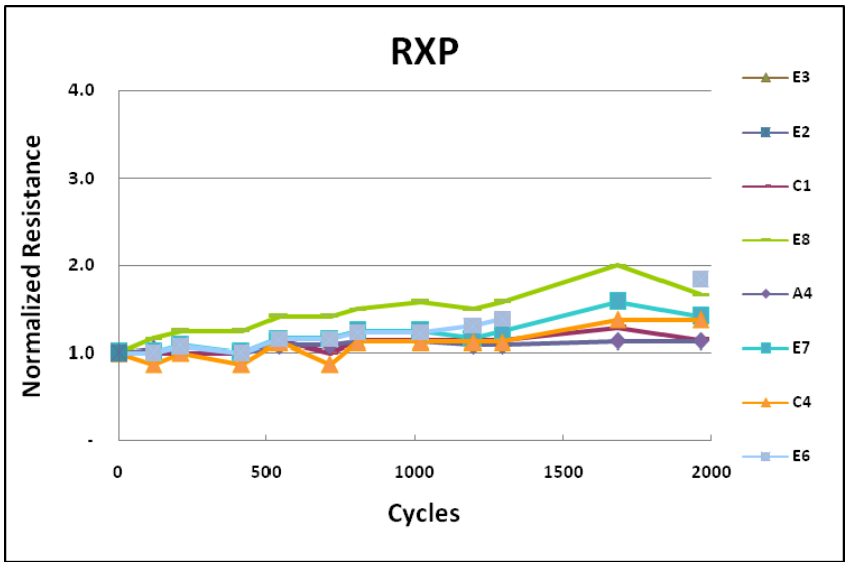


Figure 65. Normalized daisy chain resistances of test vehicle with RXP for 2000 cycles

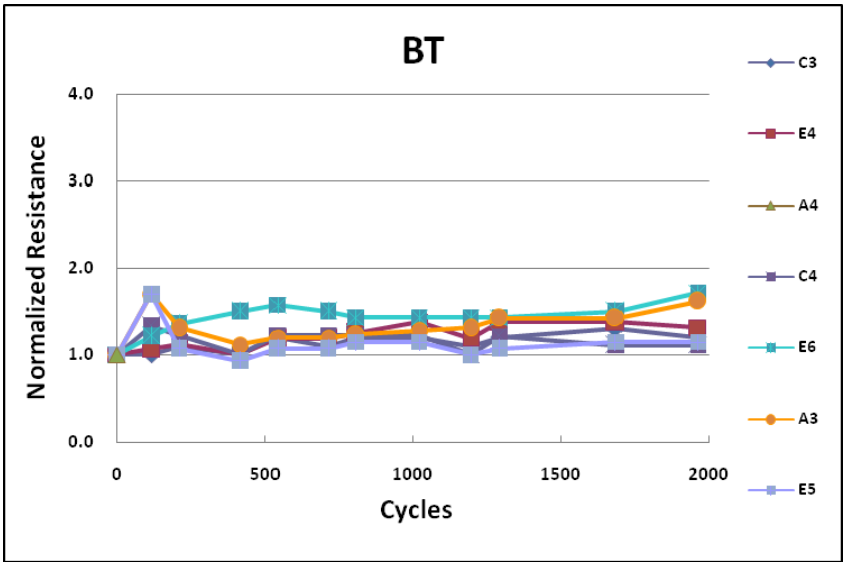


Figure 66. Normalized daisy chain resistances of test vehicle with BT for 2000 cycles

4.2 Assembly with Sufficient Load and No Tool Head Tilt

After concluding the initial reliability tests of the Cu-Cu interconnections in the area-array test vehicle, samples were assembled at Namics Corporation with sufficient assembly load and a proper tool head without tilt. The first task at Namics was to optimize the process load, which was determined to be 196N, for the area-array test vehicle with BT.

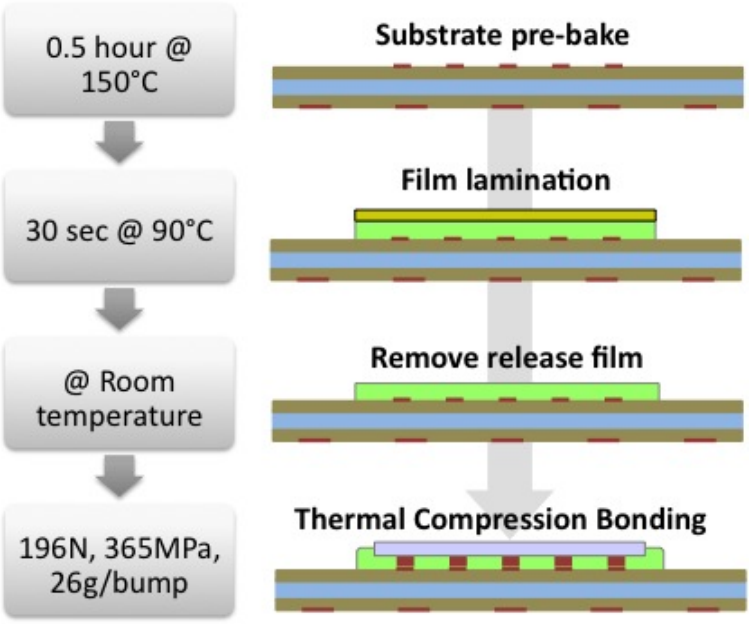


Figure 67. Process flow using BT substrates and NCF at Namics Corporation

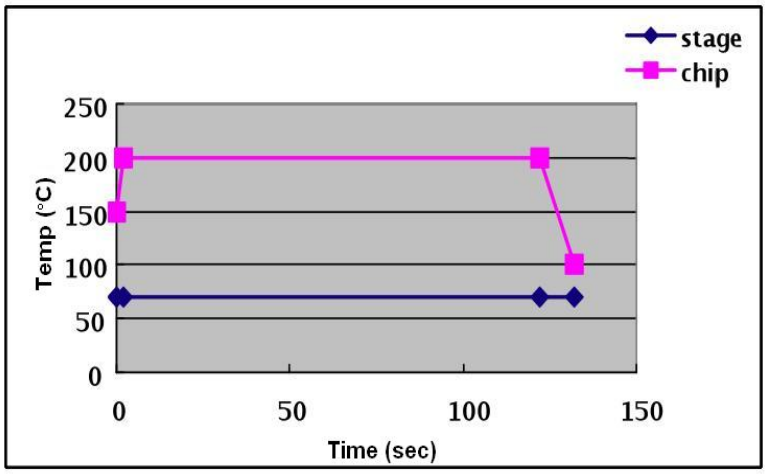


Figure 68. Temperature profile used during thermo-compression bonding at Namics Corporation

After assembly, the guidelines in Figure 58 were again followed. Good electrical yield was observed through inspection of the daisy chains, which confirmed that all the bumps in the assemblies were connected to the substrate. C-SAM images were taken and no voiding was detected. In order to verify that there was sufficient load applied during the assembly process, cross-sectional analysis was completed and proper bump-to-pad deformation was observed.

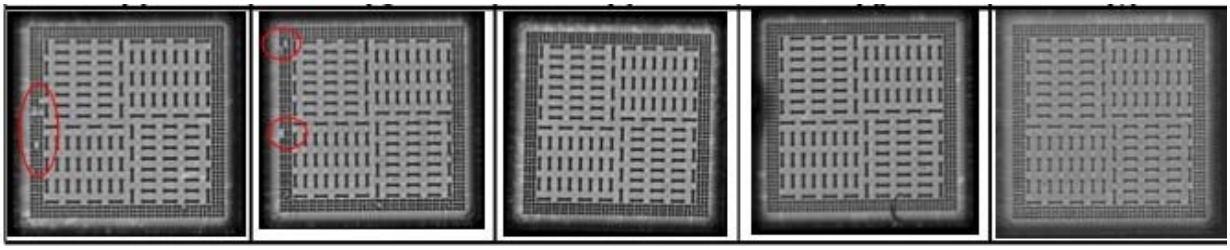


Figure 69. Final BT assemblies with good electrical yield and no voiding (red circles show missing bumps from the die side due to fabrication defects)

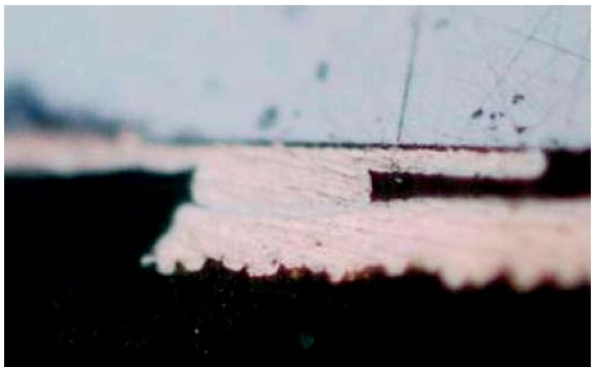


Figure 70. Cross-sectional image showing proper bump-to-pad deformation of a BT assembly with NCF

After overcoming difficulties with tilt and insufficient load, the new assemblies were analyzed for thermo-mechanical reliability. They were initially subjected to pre-conditioning, which included a baking step at 125°C for 24 hours prior to moisture sensitivity level-3 (MSL-3) at 60°C and 60% RH for 40 hours. The assemblies were then exposed to three times reflow with a peak temperature of 260°C. The pre-conditioning steps followed IPC/JEDEC Standard J-STD-020A. After pre-conditioning, C-SAM images were captured and extensive voiding was observed. Cross-sectional analysis of

these assemblies, shown in Figure 71, showed delamination between the die and NCF, which prompted a separate experiment to investigate the effect of die-surface passivation on delamination.

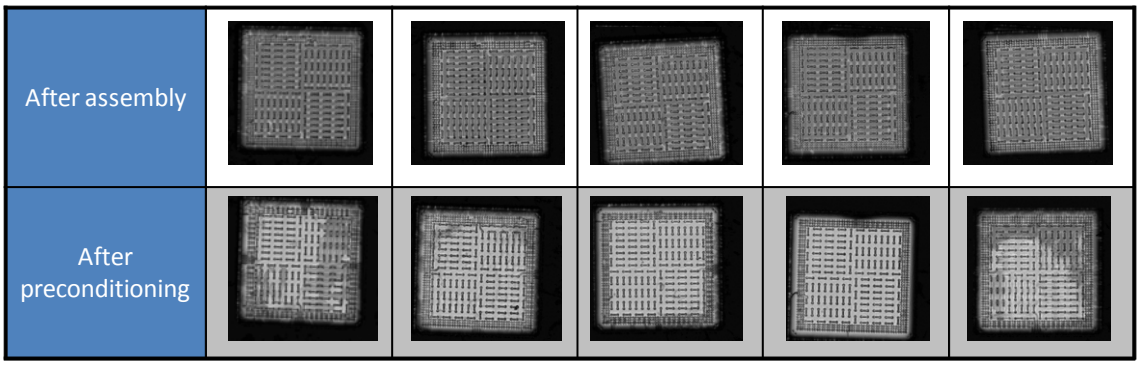
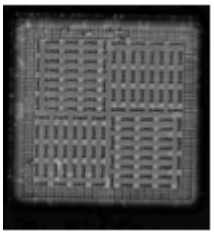
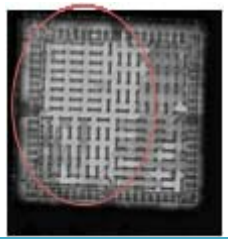
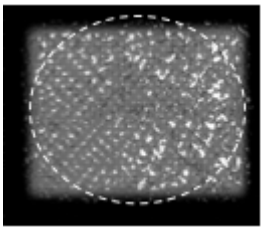
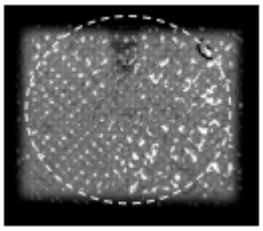


Figure 71. C-SAM images of BT samples after assembly and pre-conditioning

Figure 72. Cross-sectional analysis of BT assembly showing delamination between silicon die and NCF after pre-conditioning

An existing test vehicle with a polyimide surface passivation layer instead of SiO_2 passivation was assembled with NCF and subjected to pre-conditioning. It was observed through C-SAM images that the polyimide surface finish of the new sample assisted in relieving delamination, as shown in Table 22. These results confirmed that a passivation layer with better adhesion to NCF was necessary. Polybenzoxazole (PBO) is a possible solution for improving adhesion and relieving delamination. PBO is known for its easy processability, good temperature stability, and most importantly, good adhesion to metals and underfill resins [62].

Table 22: Effect of passivation layer on delamination after pre-conditioning

TV	After Cure	After Preconditioning Test
Underfill: NCF Surface: SiO_2		**Delamination** 
Underfill: NCF Surface: Polyimide	**Void** 	**Void** **No Delamination** 

4.3 Electromigration Analysis of Cu-Cu Interconnections

The Cu-Cu interconnections were subjected to high current and temperature stress, using the test vehicles and setup previously mentioned in Chapter 3, to evaluate electromigration resistance. The interconnections were examined under current densities of 10^4 A/cm^2 to 10^6 A/cm^2 at a temperature of 130°C. The results are shown below.

4.3.1 Electromigration Testing Results

4.3.1.1 Current Density Testing at 10^4 A/cm^2, 130°C

Electromigration testing was initially performed at a current density of 10^4 A/cm^2. The area-array assembly chosen had a stable corner daisy chain resistance of 0.9Ω. In order to connect the probe pads of the corner daisy chain to the current supply, wires were soldered to the pads and extended to the current supply. The wires chosen were made to handle high temperatures of 130°C. The addition of the wires increased the daisy chain resistance to around 1.4Ω and was dependent on the length of the wires.

The initial corner daisy chain resistance of the sample was 1.7074Ω under 70.68mA of current and 130°C. The resistance increased by 3.3% over the first 72 hours to 1.7640Ω, which was hypothesized to be due to an increase in temperature. However, the sample survived more than 800 hours without failure. There was improvement in resistance observed over time, which was confirmed through a 1.69% decrease in daisy chain resistance from 1.7640Ω to 1.7324 Ω.

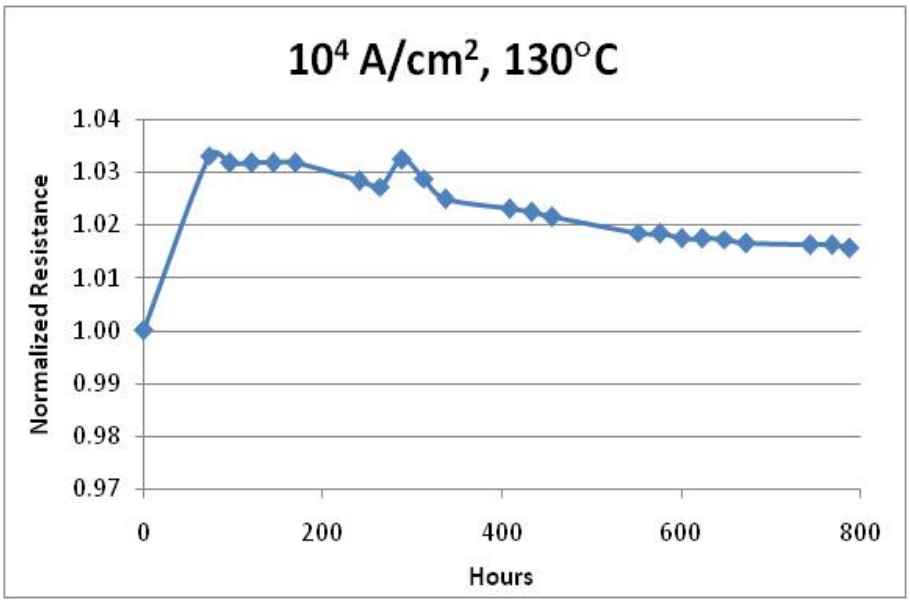


Figure 73. Plot showing area-array sample surviving ~800 hours at 10^4 A/cm^2 with an improvement in resistance over time

From previous research, the measured resistance of a single Cu-Cu bump at 15µm diameter was determined to be 7.55mΩ [36]. Using this measurement, the total resistance of the 14 bumps at 30µm diameter can be estimated at around 211.4mΩ. It is clear that the initial corner daisy chain resistance of 1.7074Ω is dominated by the Cu pad and trace resistances of the test vehicle as well as the current supply leads. This observation was consistent among all three electromigration tests.

4.3.1.2 Current Density Testing at 10^5 A/cm^2, 130°C

Electromigration testing was continued on a new assembly at a higher current density of 10^5 A/cm^2. After thermo-compression bonding was completed, a corner daisy chain was chosen with a resistance of around 0.7Ω. Once again, wires were soldered to the probe pads and extended to the current supply, which increased the resistance to around 1.1Ω. Once the Cu-Cu interconnections were subjected to 0.7068A of current and 130°C, the initial daisy chain resistance was recorded at 1.4985Ω. Within the first 111 hours, the resistance increased to 1.5252Ω. However, the sample survived more than 2800 hours without failure.

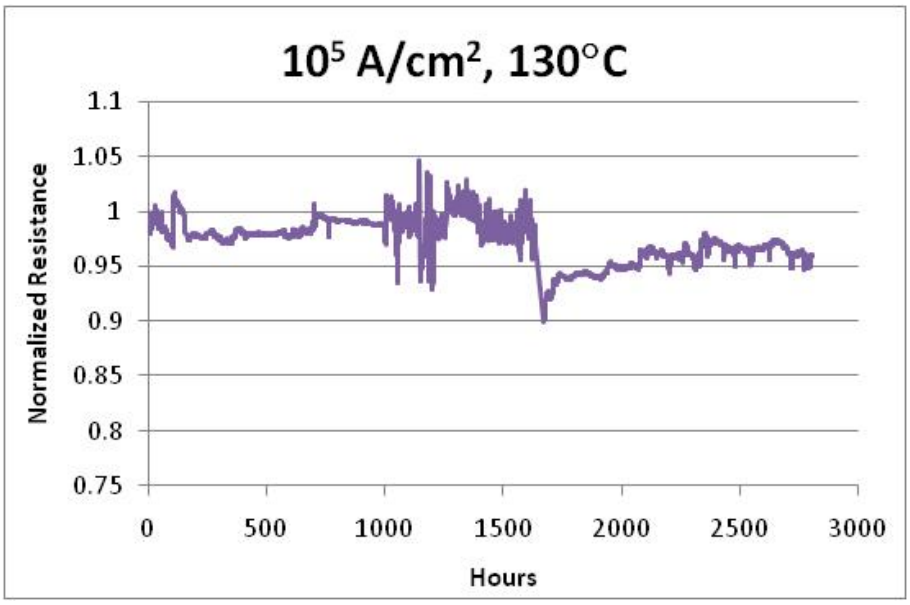


Figure 74. Plot showing area-array sample surviving >2800 hours at 10^5 A/cm^2 with an improvement in resistance over time

The plot for this sample, seen in Figure 74, had more fluctuations because an automatic data collection process was used. The result from this plot shows an improvement in resistance, similar to the data collected at 10^4 A/cm^2. However, at 10^5 A/cm^2, the corner daisy chain resistance improves even below the initial daisy chain resistance by 4% from 1.4985Ω to 1.4389Ω.

4.3.1.3 Current Density Testing at 10^6 A/cm^2, 130°C

The last test was conducted with a peripheral interconnection test vehicle. The 30µm diameter interconnections in the area-array test vehicle would require ~7A of current to achieve 10^6 A/cm^2. Therefore, the peripheral interconnection test vehicle with 15µm diameter bumps was used to achieve the same current density with a safer and lower amount of current. The corner daisy chain of the peripheral interconnection assembly consisted of a single bump and had a resistance of 0.8Ω. Adding current supply leads increased the resistance to 1.07Ω.

After applying 1.76A at 130°C, the initial daisy chain resistance was recorded as 1.00Ω. After 144 hours, the resistance reached a maximum of 1.0892Ω. The sample, nonetheless, survived for ~1100 hours without failure and showed an improvement in resistance over time. Once again, the resistance decreased below the initial daisy chain resistance. The improvement in resistance observed for all three electromigration tests suggest that the connection between the Cu pillar from the die side and Cu pad from the substrate side was improving.

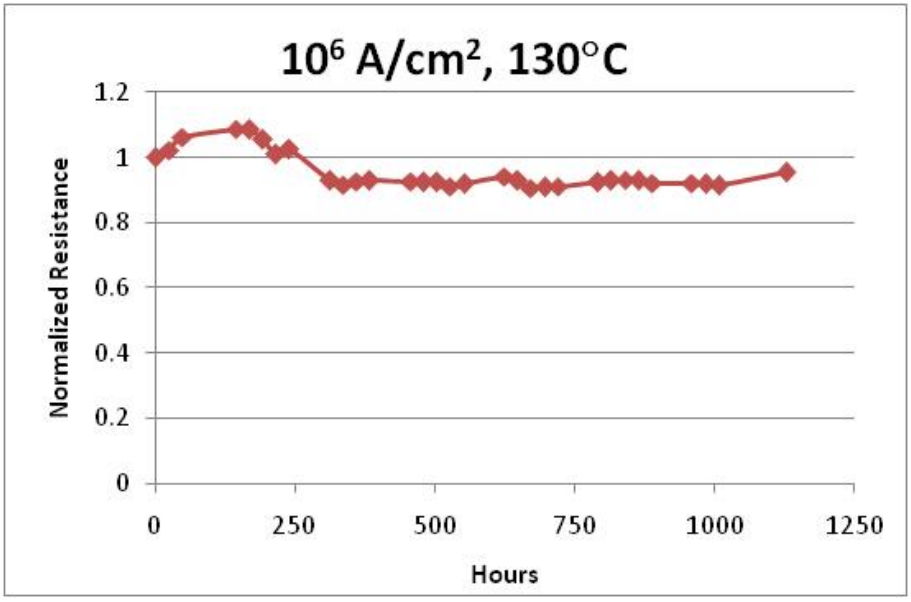


Figure 75. Plot showing peripheral interconnection sample surviving >1100 hours at 10^6 A/cm^2 with an improvement in resistance over time

The last test was attempted at 10^7 A/cm^2 with a peripheral interconnection assembly. In this test, however, the high current density and associated temperature increase caused burning of the polymer surrounding the Cu trace, as seen in Figure 76.

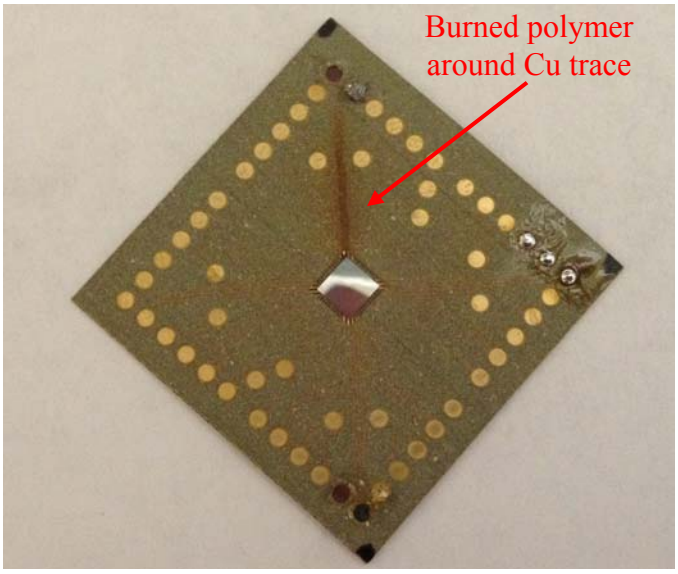


Figure 76. Image showing burned polymer around Cu trace after applying 10^7 A/cm^2 current density

4.3.2 Joule Heating Experiment

To investigate the increase in temperature of the Cu-Cu interconnections due to joule heating, another sample with peripheral interconnections was subjected to different currents at room temperature. A thermal infrared camera was used to determine the change in bump temperature. The IR camera detects infrared energy and converts it into an electronic signal in order to produce a thermal image [63].

Wires were initially soldered to the corner daisy chain of the sample, consisting of a single bump, and then connected to a current supply. The sample was positioned on a stage below the infrared camera and the temperature of the stage was set to 20.1°C. The thermal image of the bump was then captured as the current was slowly increased to 0.01A, 0.1A, 0.2A, 0.3A, 1A, and 2A. The image in Figure 77 illustrates an overlapped die and substrate design, which shows the location of the corner daisy chain with the

single Cu-Cu interconnection. The design depicts the area upon which the IR camera was focused, as seen in Figure 78. Additionally, Figure 78 displays the emissivity, indicating the amount of radiation emitted by the different structures in the sample.

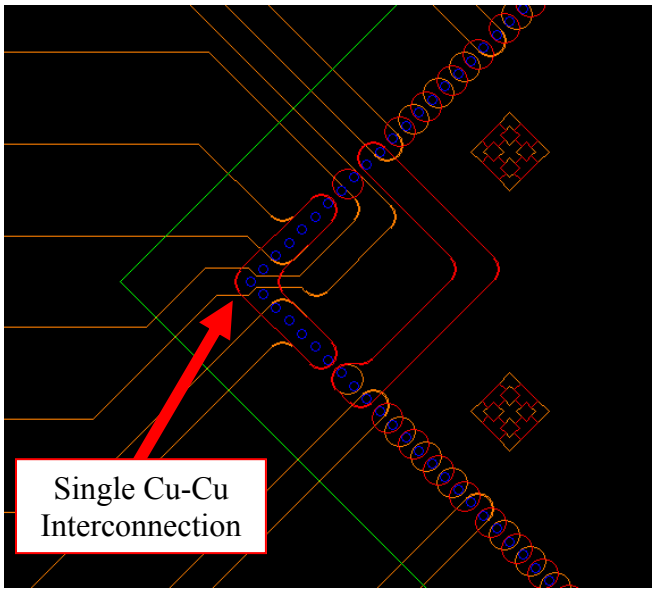


Figure 77. Overlapped die and substrate design showing the single corner bump which current was applied to

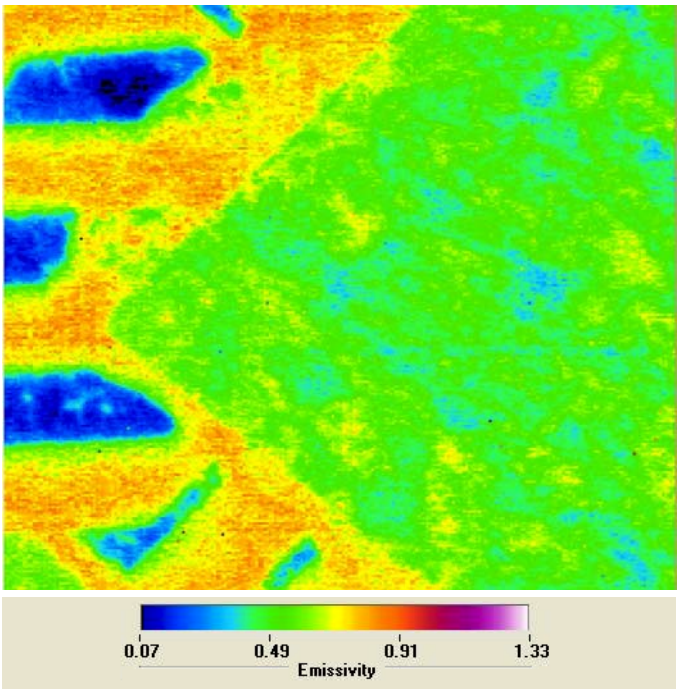


Figure 78. IR image of the sample displaying emissivity and the different structures such as the Cu bumps and Cu traces

The plot in Figure 79 shows the increase in bump temperature as a function of applied current. The bump temperature at 2A is within the maximum temperature range for high power applications, which is 200°C [5]. An embedded power management IC (PMIC), for example, requires a current carrying capability of 1A with a maximum junction temperature of 150°C [64], proving the Cu-Cu interconnections suitability for high power applications.

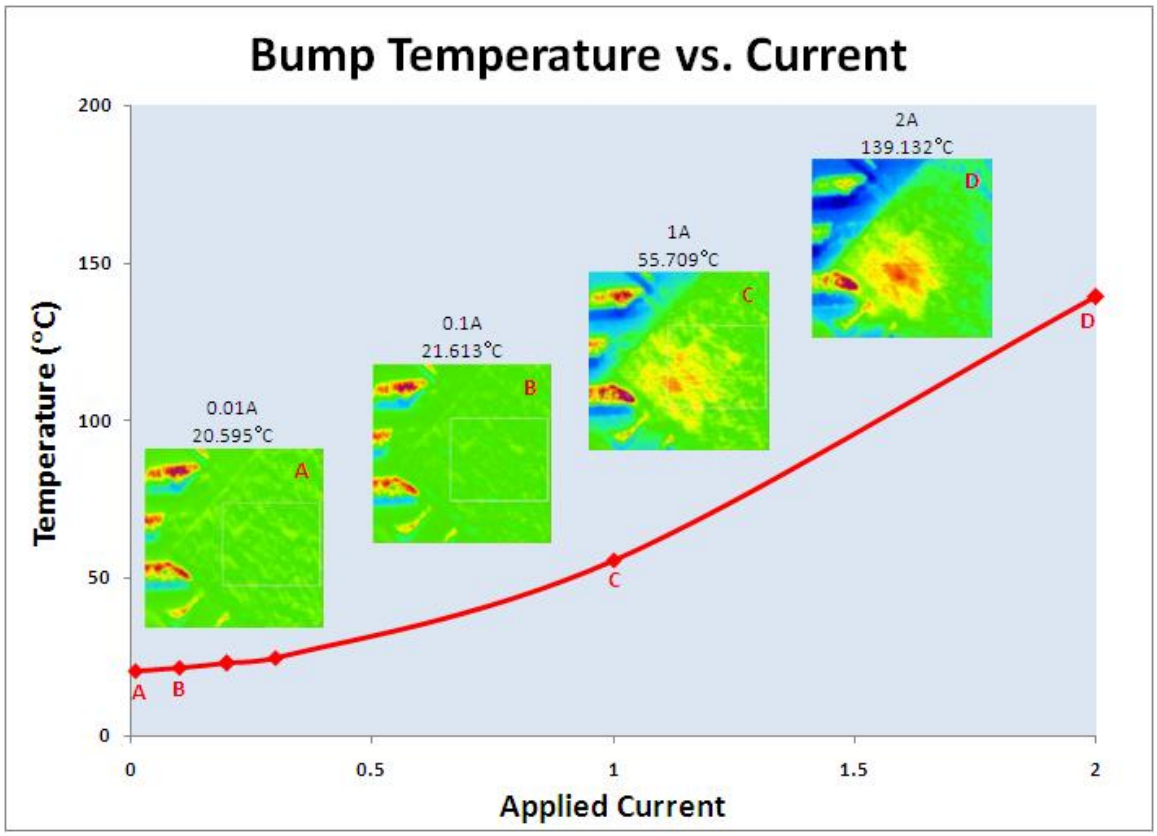


Figure 79. The increase in bump temperature due to joule heating with respect to the applied current

Another 3D model was constructed with ANSYS, using the same design parameters mentioned in Chapter 2, to confirm the increase in bump temperature at 2A of input current. The Cu-Cu interconnection was created at 15µm diameter and 15µm height to model the bump in the peripheral interconnection test vehicle. The image in Figure 80 shows that the maximum bump temperature was around 418K, equivalent to 145°C,

which is close to the experimental result and is still within the temperature range for high power applications.

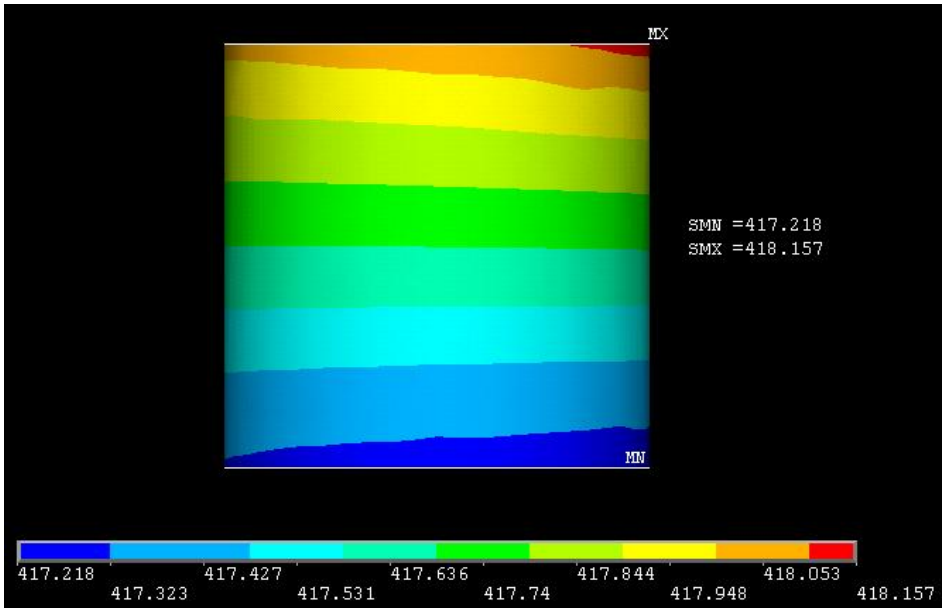


Figure 80. ANSYS model showing temperature distribution of 15µm diameter Cu bump

4.4 Cu-Cu Interconnections Discussion

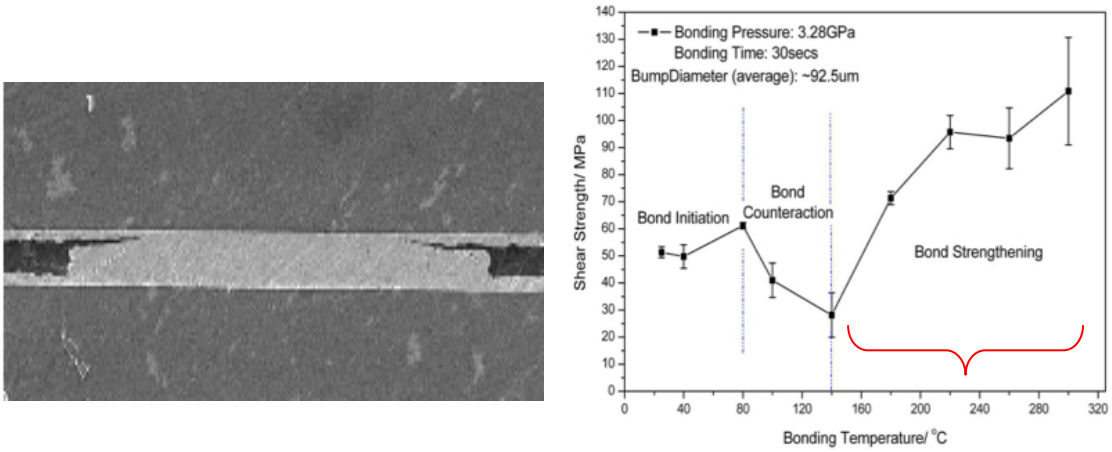
Cu-Cu interconnections, bonded at low temperature, are an ideal candidate for next generation flip chip packages. Copper's superior electrical and thermal conductivity enable it to overcome the barriers associated with electromigration at small bump dimensions. The ANSYS results obtained from this research indicate the Cu-Cu interconnections ability to withstand current crowding and joule heating effects under 1A of current stress. Experimental results prove the high electromigration resistance of the Cu-Cu interconnections at current densities up to 10^6 A/cm^2. In the future, further analysis can be done by using Focused Ion Beam (FIB) microscopy to examine the bump-to-pad interface of the Cu-Cu interconnections, after high current and temperature stressing.

Equation 9 was used to determine the lifetime of the Cu-Cu interconnections at 10^6 A/cm^2. The peak current density was obtained from ANSYS in order to properly take

into account the current crowding factor. The temperature was established as 130°C and ΔT was extrapolated from the joule heating experiment to determine the increase in bump temperature at 1.76A. Literature states that the current density exponent, n, for Cu is 1 [65-66] and the activation energy, E_a, was chosen as 1eV [53]. Using the mentioned values, the MTTF was calculated to be 956 hours. This value was close to the 1100 hours observed during experimental testing at 10^6 A/cm^2.

As mentioned, one of the technical challenges of achieving high electromigration resistance with the proposed Cu-Cu interconnection technology was the low bonding temperature at 180°C. The Cu-Cu interconnections do not exhibit interfacial atomic diffusion, resulting in a non-metallurgical or mechanical bond [36]. The following literature suggests that thermal-induced diffusion and grain growth is required to create a homogenous Cu-Cu structure with no distinguishable interface. This is usually obtained through high temperature bonding and annealing. However, the current research suggests that a homogenous structure is not required to achieve high yield and reliability.

X. F. Ang et al. [67] reported that a strong Cu-Cu bond can be achieved at bonding temperatures greater than 140°C, but with a high applied load. Dies with electroplated Cu bumps were bonded to substrates after both were treated with hydrochloric acid for 30 seconds. Thermo-compression bonding was initially completed at room temperature with 3.28GPa of pressure, which completely removed the bonding interface and created a homogeneous structure. Further examination established that high bonding strengths could also be achieved at temperatures of 180-300°C.



(a) **(b)**

Figure 81. (a) Image showing disappearance of the bonding interface after Cu-Cu thermo-compression bonding at room temperature and high load; (b) Graph showing measured shear strengths at different bonding temperatures [67]

W. Ruythooren et al. at IMEC [68] also witnessed 100% yield and good resistance at bonding temperatures of around 230°C for 15µm bumps. Their strategy included preparing the electroplated Cu surfaces by diamond bit cutting to attain an average surface roughness, R_a, of 9nm. Fujitsu [69] took a similar approach in which the Cu bumps were planarized with a diamond bit to create an amorphous-like layer at the surface. This assisted in creating a monolithic Cu-Cu interface at temperatures of 200-250°C. Sematech [70] investigated Cu-Cu bonding at wafer level by demonstrating Cu-Cu thermo-compression bonding at 300°C with an annealing step at 400°C. The original bonding interface for their Cu-Cu structure had disappeared due to diffusion and grain growth, causing the layers to merge and a homogeneous layer to be attained.

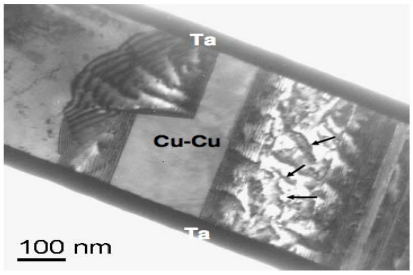
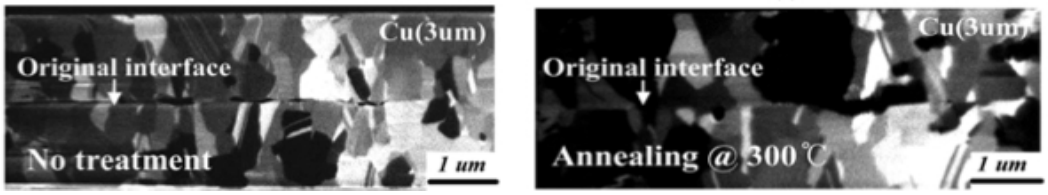


Figure 82. After Cu-Cu bonding at 300°C and annealing at 400°C, a homogenous layer was obtained through diffusion and grain growth [70]

A study by E. J. Jang et al. [71] experimented with Cu-Cu bonding at different temperatures. At a bonding temperature of 300°C, the bonding interface between two Cu films was still visible. However, after an additional annealing step at 250°C, the interface started to disappear and at 300°C a clean Cu bonded layer was achieved.



(a) **(b)**

Figure 83. (a) Distinguishable Cu-Cu interface observed after bonding at 300°C which (b) disappears after a 300°C annealing step [71]

Lastly, a thorough analysis was completed by K. N. Chen et al. [72] from MIT regarding Cu wafer bonding at different bonding and annealing temperatures. The authors confirmed that grain growth could be achieved via thermo-compression bonding at 350°C for 30 minutes in combination with a 350°C annealing step for 60 minutes. Additionally, K. N. Chen et al. evaluated the bonding characteristics at other conditions, as shown below, to meet the demands of the industry for a fast and low temperature process.

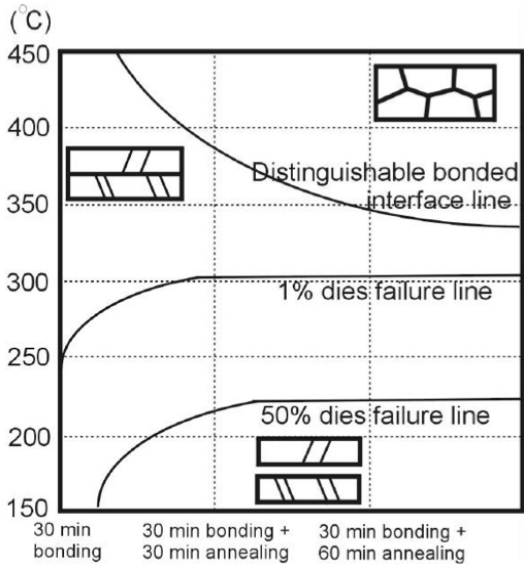


Figure 84. Morphology and strength map for Cu wafer bonding under different bonding temperatures and conditions [72]

Bonding Duration / Bonding Temperature	30 min bonding	30 min bonding + 30 min annealing	30 min bonding + 60 min annealing
400 C	0 % dies failed	0 % dies failed	0 % dies failed
350 C	0 % dies failed	0 % dies failed	0 % dies failed
300 C	0 % dies failed	5 % dies failed	4 % dies failed
250 C	1 % dies failed	21 % dies failed	22 % dies failed
200 C	18 % dies failed	86 % dies failed	75 % dies failed
150 C	37 % dies failed	90 % dies failed	96 % dies failed

Figure 85. Percentage of failed dies at different bonding conditions after dicing [72]

The study at MIT established that a Cu layer with excellent bonding can be obtained at temperatures greater than 350°C with an additional annealing step. Nonetheless, Figure 85 confirms that even though a homogeneous Cu-Cu interface is not formed at lower temperatures, high bonding yield can still be attained. These findings support the research presented within this thesis, proving that Cu-Cu thermo-compression bonding at 180°C can produce interconnections with high yield, high thermo-mechanical reliability, and high electromigration resistance.

Three distinct characteristics of the Cu-Cu interconnection technology allow for this high reliability: 1) proper bump-to-pad deformation, 2) ultra-thin NCF, and 3) ENEPIG surface finish. Obtaining proper deformation of bump-to-pad after assembly is crucial in enabling a good electrical connection and using an ultra-thin NCF further assists in maintaining a strong bond after thermo-compression bonding. The ENEPIG surface finish creates an Au-Au interface, which prevents Cu oxidation and promotes a reliable contact bond with low resistance. These three contributing factors have assisted in the achievement of a robust and versatile Cu-Cu interconnection technique.

CHAPTER 5

SUMMARY AND FUTURE WORK

This chapter provides a summary of the research completed to validate the high thermo-mechanical reliability and explore the electromigration resistance of the Cu-Cu interconnections. The conclusion reached from this research is discussed and recommendations for future work are suggested.

5.1 Summary

The future of microelectronic systems is dependent on innovations in electronics packaging to enable ultra-miniaturization and high functional density. Flip chip packaging is used in a variety of applications that require high computing capabilities and wireless access to data-rich content, such as cell phones and graphical processing units (GPU). In order to continue the constant progression of these applications, new interconnection technologies need to be developed at ultra-fine pitch, low stand-off height, and with high current carrying capability.

Solder bumps are the most common flip chip interconnection method, but forcing this technology to finer pitch has created concerns due to high current densities that cause electromigration. Flip chip solder bumps undergo various electromigration failure mechanisms such as current crowding, joule heating, UBM dissolution, and IMC formation. Furthermore, the current density threshold for electromigration of solder bumps is 10^4 A/cm^2. This is a serious reliability concern considering that flip chip design rules require solder bumps to handle this amount of current density in the near future. To overcome the pitch-scaling limitations of solder bumps due to electromigration, this research focused on exploring the electromigration resistance of 30μm Cu-Cu interconnections as a replacement for solder. Cu was chosen due its high melting point

and high threshold for electromigration at 10^6 A/cm^2. Furthermore, the all-copper interconnection system decreases the chance of flux divergence which induces failures.

FEM was used to compare the current crowding and joule heating effects of the Cu-Cu interconnection to two existing flip chip interconnections, Cu pillar with solder and Pb-free solder. The peak current density, current crowding ratio, joule heating, and maximum bump temperature were evaluated for all three interconnections. The Cu-Cu interconnection was able to effectively dissipate the heat generated by joule heating due to current crowding at an input current of 1A.

Experimental testing was completed after design and fabrication of the test vehicle. The die consisted of 30μm diameter Cu-Cu interconnections and was fabricated using a semi-additive process. The substrate was designed with 24 probe pads to measure the resistances of the 16 daisy chains during TCT and electromigration testing. A subtractive etching process was used to fabricate the substrates with both BT and RXP.

After fabrication, samples were assembled using thermo-compression bonding with ultra-thin NCF at 180°C. Despite insufficient load and delamination, area-array assemblies passed more than 2000 cycles of TCT. After subjecting the Cu-Cu interconnections to pre-conditioning, however, extreme voiding was observed. Cross-sectioning proved that there was delamination at the die and NCF interface due to the lack of an organic passivation layer. PBO was suggested as a potential solution for improving adhesion between the die and NCF.

The Cu-Cu interconnections were then examined under high current densities ranging from 10^4 A/cm^2 to 10^6 A/cm^2 at a temperature of 130°C. The first test at 10^4 A/cm^2 showed no failure for more than 800 hours and improvement in resistance was observed over time. At 10^5 A/cm^2, there were no failures observed for more than 2800 hours and at the highest current density of 10^6 A/cm^2, there were no failures observed for more than 1100 hours. At both 10^5 A/cm^2 and 10^6 A/cm^2, the resistance decreased below the initial daisy chain recorded at the beginning of testing. A joule heating experiment

was also conducted to observe the increase in bump temperature at different input currents, which demonstrated the potential of the Cu-Cu interconnections to be used for high power applications.

Literature states that a bonding temperature greater than 300°C is necessary to transform a Cu-Cu interface to a homogenous layer. However, this research confirms that a homogeneous layer, or metallurgical bond, is not required for obtaining high thermo-mechanical and electromigration reliability.

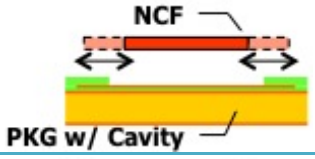
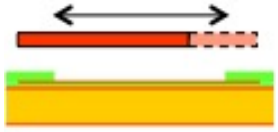
5.2 Future Work

The proposed Cu-Cu interconnection technology has previously been established as highly reliable with peripheral bumps at 30μm pitch [36]. This research further advanced the Cu-Cu interconnection technique by demonstrating high electromigration resistance at small diameter and low bonding temperature. Given that the phenomenon of electromigration is a growing concern at small interconnection dimensions, additional research can be completed to further prove the high reliability of the Cu-Cu interconnections:

- After electromigration testing, the bump-to-pad interface of the Cu-Cu interconnection should be analyzed using FIB microscopy to understand the change in microstructure under high current and temperature stress.
- The Cu-Cu interconnections can be investigated for absolute current carrying capability and also thermal issues that are associated with these high currents.
- In order to prove that Cu-Cu interconnections are more electromigration resistant than solder capped Cu pillar interconnections, CuSn interconnections at small diameter can be fabricated and tested under the same conditions used in this research. Literature suggests that current densities higher than 10^4 A/cm^2 has not been completed for existing interconnection techniques, so this analysis would be beneficial in establishing the push for non-solder based interconnections.

- Joule heating was investigated in this research but can be further analyzed by incorporating a TaN temperature sensor to the test vehicle, allowing for in situ measurements of the actual device temperature.
- In the past and present research work, both ENIG and ENEPIG surface finishes were used to prevent Cu oxidation from occurring. Electromigration analysis should be completed on bare Cu-Cu interconnections, without a surface finish, to explore the possibility of a simpler and low cost process.
- A simpler process can be evaluated for thermo-compression bonding using b-stageable no-flow underfill (BNUF). The following table demonstrates the benefits of using this material. Thermo-mechanical reliability along with electromigration testing should be completed for assemblies with BNUF.

Table 23. Benefits of BNUF over NCF

Compatible for Cavity	NCF		BNUF
Size Control		Need precision cut	By dispensing pattern
Alignment Control		Need film alignment	Not required
Thickness Control		Need to make different thickness film	By dispensing volume

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